

## RAJ NAIR

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### EXECUTIVE SUMMARY

Raj has **22+** years experience in VLSI & Electronics Systems Design, Manufacture & Management. A significant portion of this time has been and continues to be in advanced analog, mixed-signal, custom digital circuits and VLSI design and manufacture. He has been an individual contributor and in senior management roles from project definition to product delivery. He has **40+** issued US/international **patents**.

His assignments include L&T (a premier engineering company in India's private sector), Intel Corporation, numerous faculty / research positions, and a number of start-up and small companies as contributor, advisor, or in senior management and founding roles. He is a prolific inventor and creator of industry-first products.

At L&T Bangalore Works in 1987, Raj developed the earth-moving industry's first electronic, operator-free, excavator test system that he then converted into a remote control for such machines. He conducted research into online detection of soil compaction in vibratory compactors. At L&T-Gould, he developed a thermal strip chart recorder cycling power sequentially from an existing power delivery system to thermal heaters.

Raj was responsible for conceiving, designing, and delivering the industry's first on-chip-integrated low-cost, high-bandwidth distributed voltage regulation for micro-controllers in 1995 resulting in 4 patents. This innovation was implemented in at least two Intel® Corporation products, 80296SB™ and 80196NV™. Subsequent to that work Raj was responsible for the analog signal path architecture as well as a performance critical double sampler circuit block of Intel's first production-worthy CMOS image sensor chip 'Eye2' in 1997. His work contributed to Intel's Decatur™ camera product and the *digital imaging revolution*.

Raj conducted research at Intel labs and was instrumental in developing an on-chip depletion/accumulation mode decoupling capacitor strategy, discovering and patenting its noise suppression benefits due to voltage dependency of capacitance. This technology has been adopted in all of Intel's 130nm products and beyond. Raj was the analog circuit design expert in the research team developing adaptive body-biasing techniques for leakage reduction; he solely owned clock generation, distribution as well as global and local power delivery and packaging of a ground-breaking 180nm 28.5GB/s non-blocking crossbar 1cm<sup>2</sup> chip. This chip, designed for 1GHz operation, was tested successfully at 2GHz. Raj initiated research efforts into high-speed signaling (10Gb/s) while at Intel labs. He conceived and patented negative-hysteresis techniques in high-speed receivers that reduced receiver jitter and improved BER. He participated in strategic technology roadmap activity for Intel Corporation & advised an FRAM startup effort.

Raj was responsible for identification and corporate-wide communication of scaling related microprocessor package attribute trends at Intel. He was responsible for the development and corporate-wide communication of integrated CMOS regulator concepts pursued by Intel as a promising new technology. Raj has been an invited contributor of papers to both Intel's ATTJ and ITJ journals.

**Founding ComLSI** in Jan. 2003, Raj successfully increased annual revenue at this Mesa, AZ based startup specializing in Analog Design & consultation. He led a global team of experts implementing a 30m, 7.5Gb/s DVI/HDMI cable link in 180nm CMOS employing proprietary low-power true-differential signaling for long reach and improved bit-error rates exceeding DVI/HDMI specifications. Raj currently heads [Anasim](#) Corp., a spin-off, founded 09/2006, commercializing the EDA industry's first power-integrity-aware Floor Planner. He is engaged in writing/compiling a **book** on IC power integrity invited by Pearson Education.

Raj initiated the Phoenix chapter and co-chaired the AZ Nanotechnology Cluster, an organization promoting entrepreneurship and job creation in AZ, from 2004 to early 2006. He has won recognition by the State of Arizona through an AZFAST grant, and has been invited to present at *SoC 2007, NanoTech 2008 and NanoEquity 2008*. Please see [www.comlsi.com](http://www.comlsi.com) and [www.anasim.com](http://www.anasim.com) for additional information.