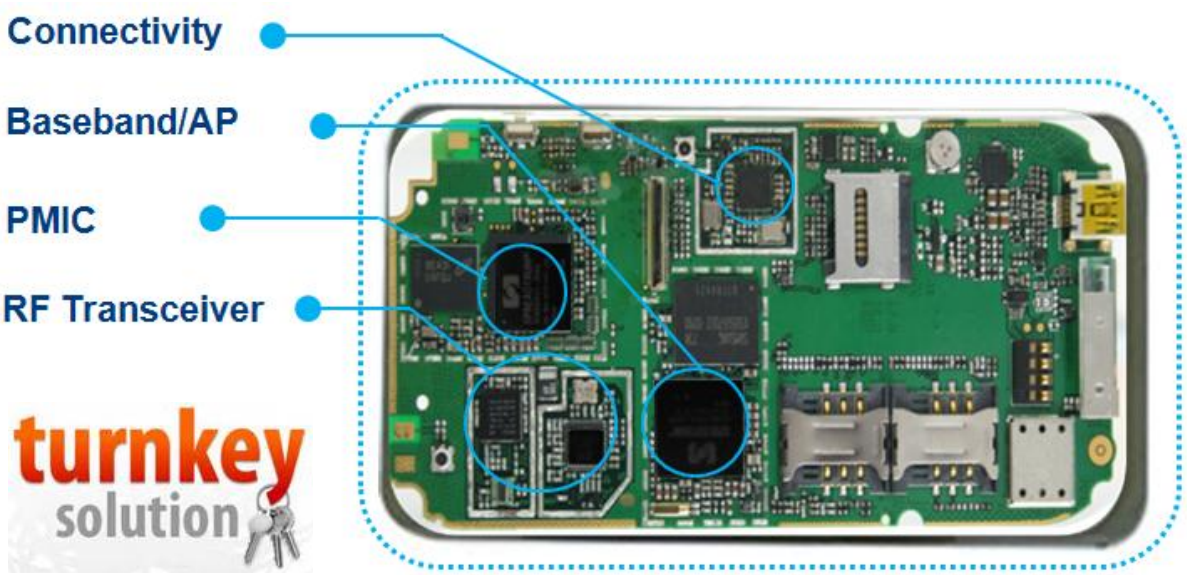
Holonomic Power Integrity Signoff Methodology of Mobile Baseband Processor

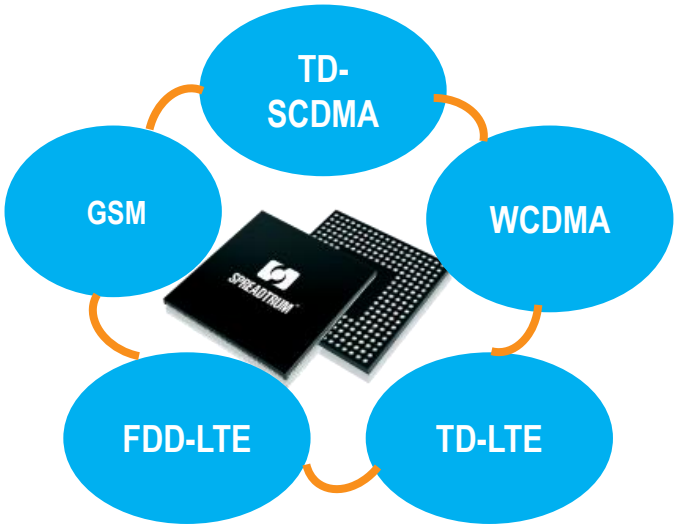
Steven Guo
Deputy Director
IC-Packaging Codesign
Aug 5,2014

展讯通信® SPREADTRUM

cadence®

Spreadtrum and Product Introduction





GSM/EDGE/TD-SCDMA/WCDMA/TD-LTE/FDD-LTE

Feature Phone /Smart Phone/Tablet / Datacard

紫光集团 TSINGHUA UNIGROUP

SPREADTRUM®

cadence®

Mobile Devices, Today & Tomorrow (I)

Lifelike Graphics

Larger Display

Better User Experier

High-Speed Connectivity

3G/4G/5G

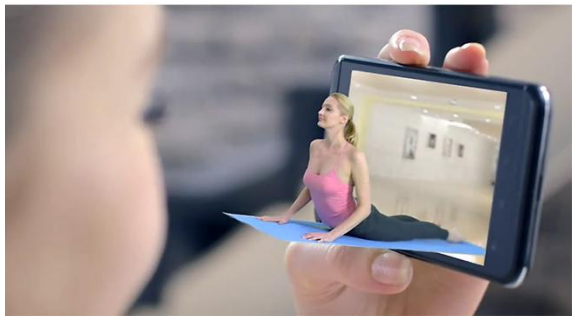
Smarter Features

Biometrics/

Health/Medical

Computing Everywhere

Multi-Core Processing



cadence

Mobile Devices, Today & Tomorrow (II)

Higher graphic resolution
Heavier application

HD: 1280x720

2K: 1920x1080

4K: 3840x2160

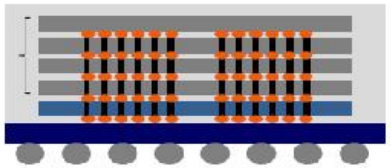
8K: 7680x4320

More density, higher band-width

LPDDR3 @2ch x32 x1600Mbps @12.8GBps

LPDDR4 @4ch x32 x3200Mbps @51.2GBps

Denisty:16GB/24GB/32GB



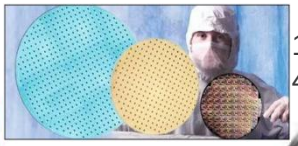
Technology

x64 @multi-GHz

Quad Core…

28nm/16nm/10nm

Less Power,
Always-on & Connected



18/12/8 inch

450/300/200mm

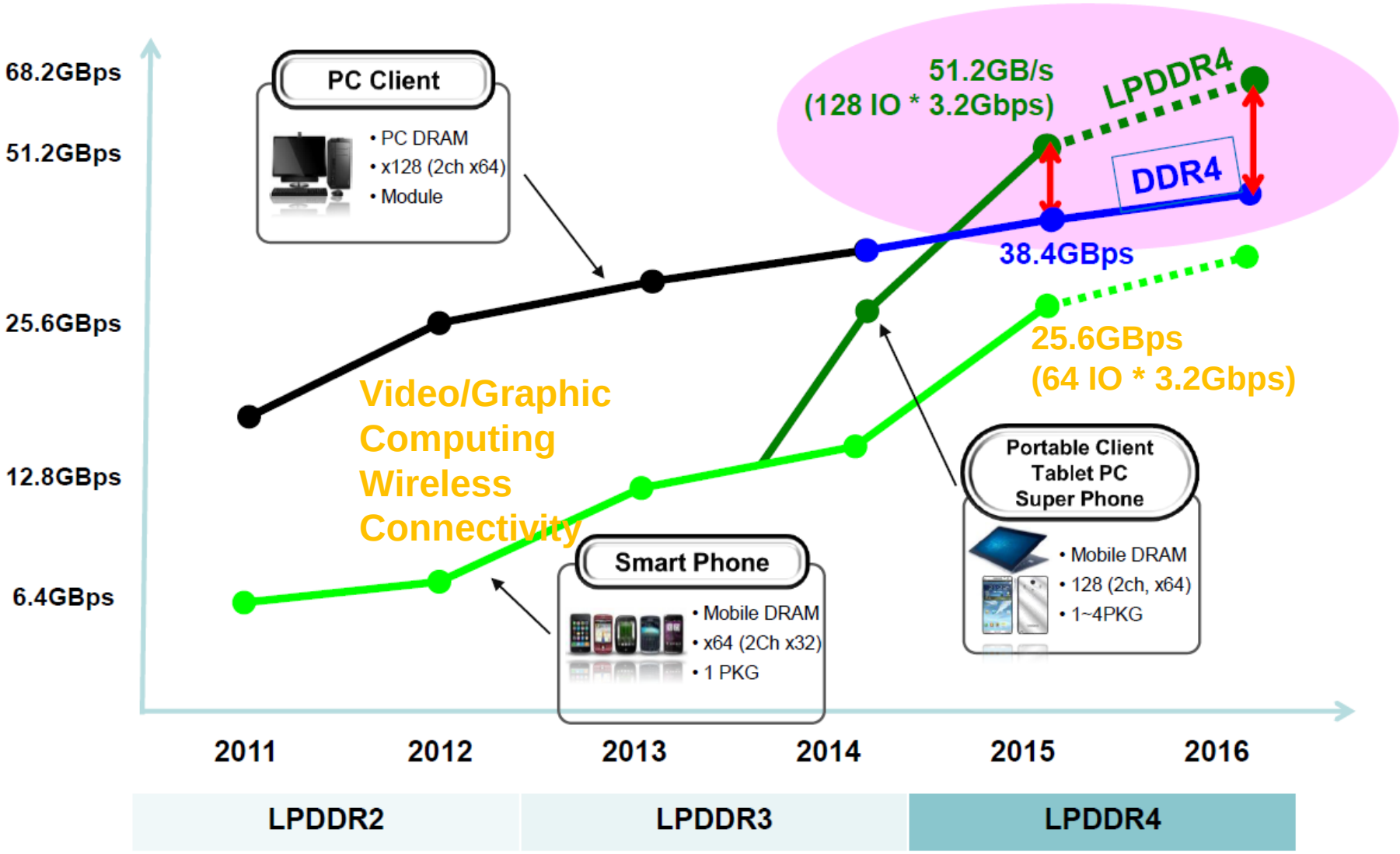
Thinner and Lighter

11.2 9.3 9.2 7.1 6.2 5.8….

(mm)

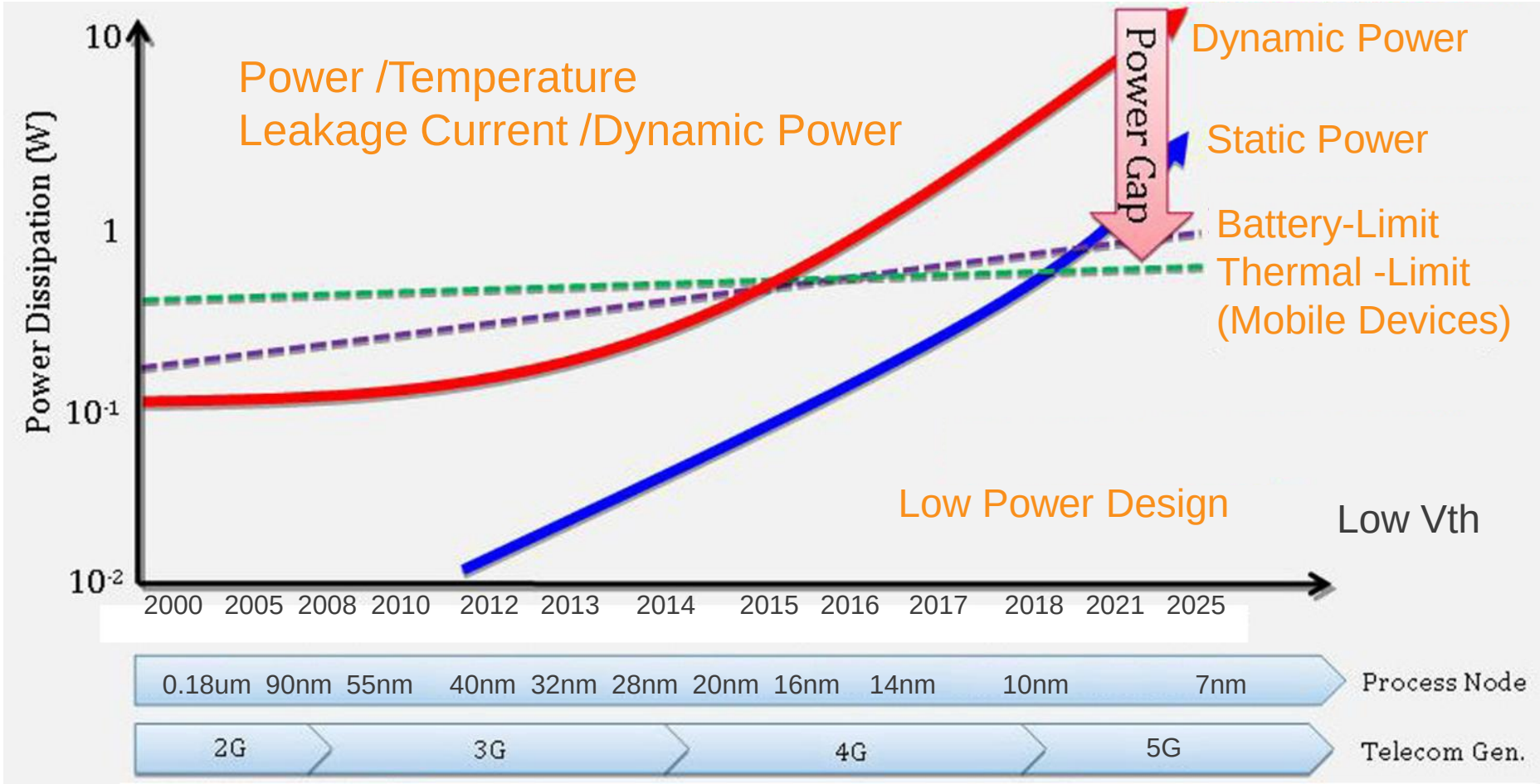
cadence

Mobile DRAM will Exceed PC DRAM Performance



cadence

Lower Power Design and Power Trend



cadence

Power Signoff Challenges of Mobile Chips

COST DOWN

High Performance

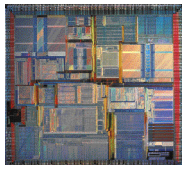
User Experience

Less Design Margin

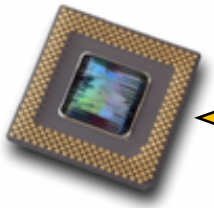
VDD: 0.9V
L * di /dt
Lower Vt
Larger Leakage

cadence

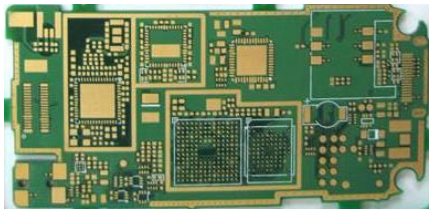
Power Integrity Analysis Collaborating Across Team



IC Power Analysis Designer



Package Electrical Analysis Engineer

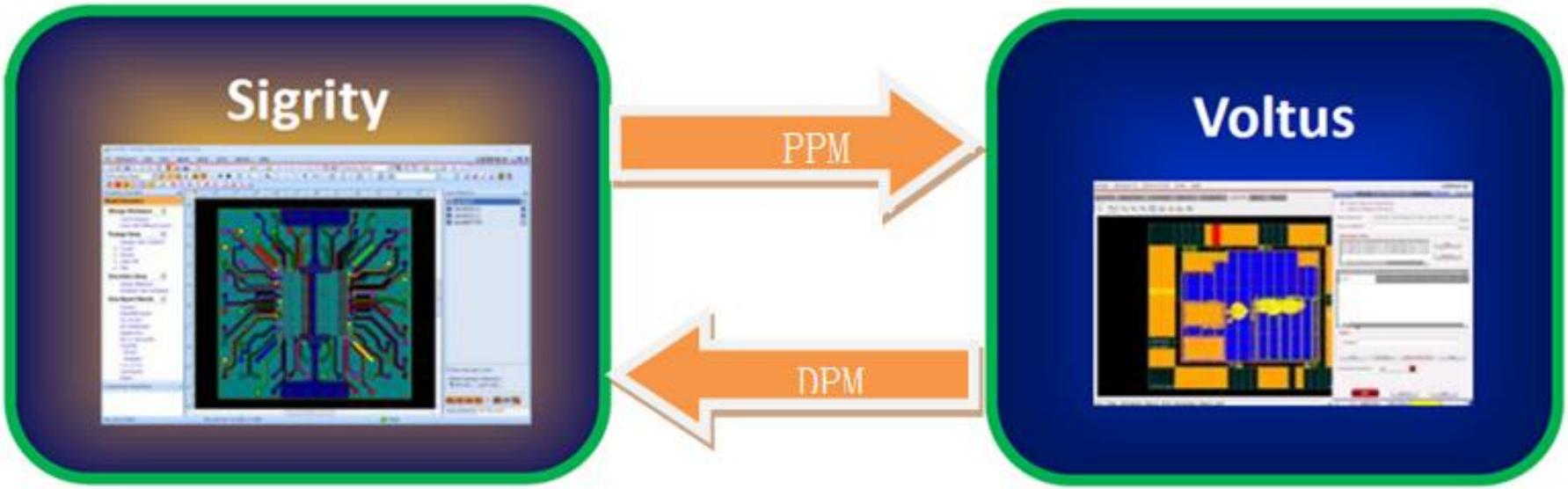


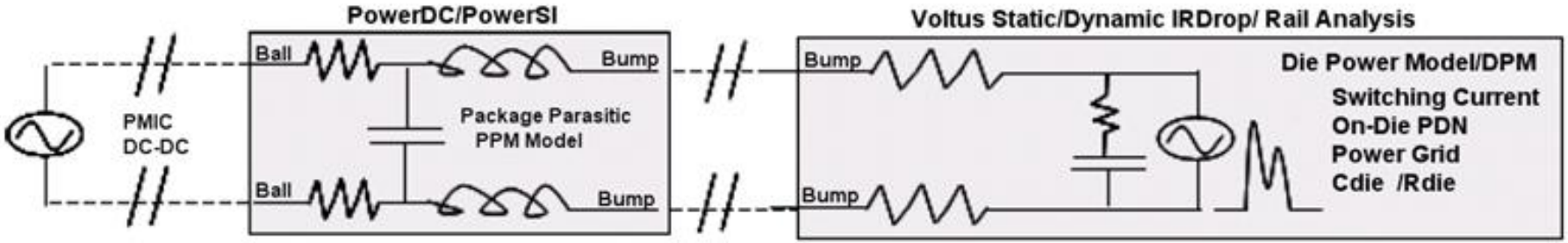
System Electrical Analysis Engineer

CoWork

PI is not just IC Designer's Job

System/IC-Centric PI Co-simulation





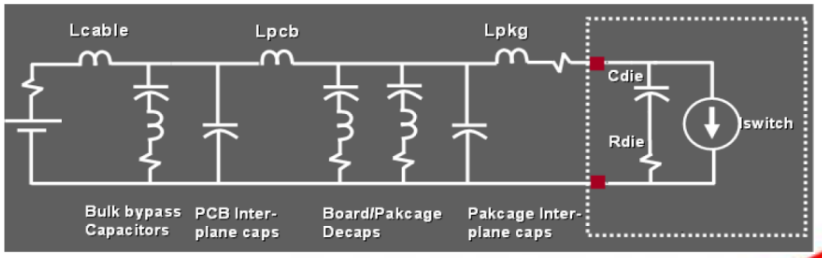
PMIC/DC-DC
PCB/Decap

On-Package IR-Drop
Source: Ball
Sink: Bump

On-Chip IR-Drop
Source : Bump
Sink: Macros /Memory
Standard Cell

cadence

Schematic representation of a Chip/System Co-simulation



DC-DC Decap

PPM
Static: Pure-R pin network
Dynamic: RLCK pin network

PCB

Ball

Package

100um

RDL Layer

Bump

Mx Layer

Cdie

C3

C1

C2

Default cap in this area

This region is switched off

I3

I1

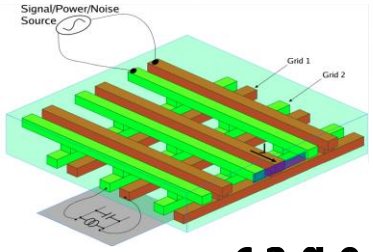
I2

Standard /Memory

Cells/ Poly/Circuit

Switching Current

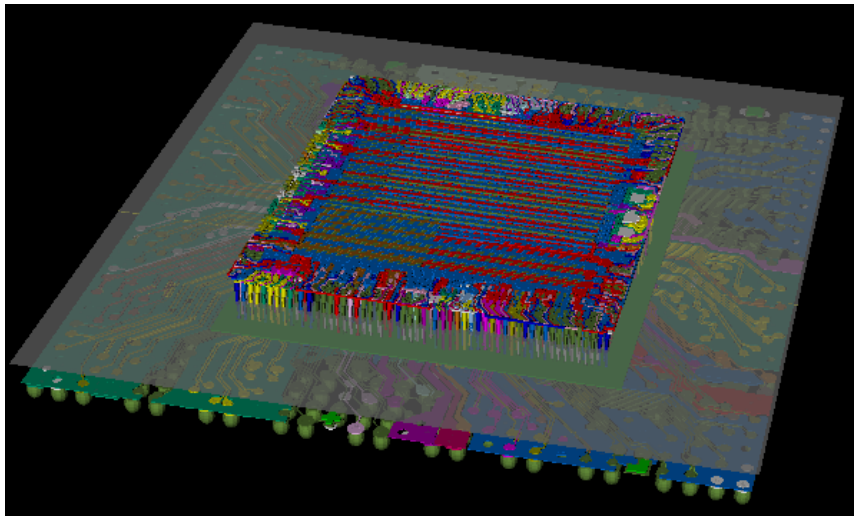
DPM
DC: Die Current /DC
AC: Die Current /PWL

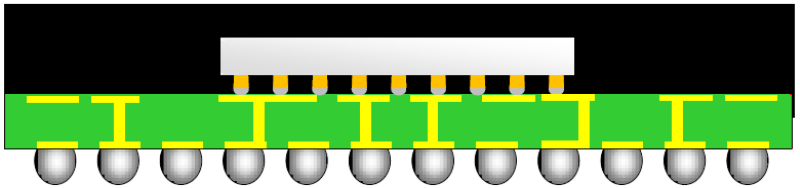


cadence®

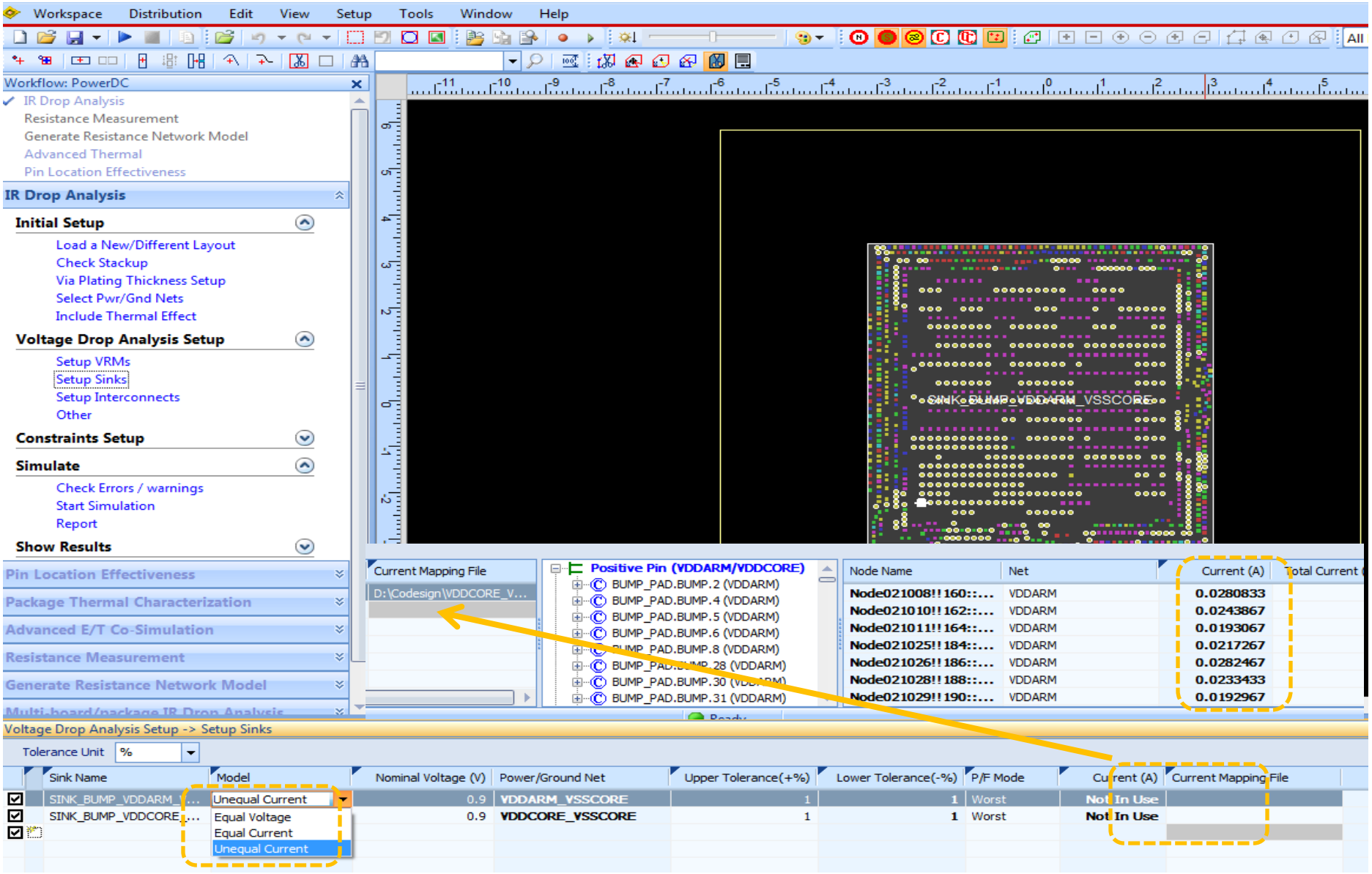
Flipchip Baseband /Application Processor Case

- Ball: 492
- Bumps: 1537
- Power Net: VDDCORE 0.9V (TT)
- VDDARM 1.0V (TT)
- Ground Net: VSSCORE



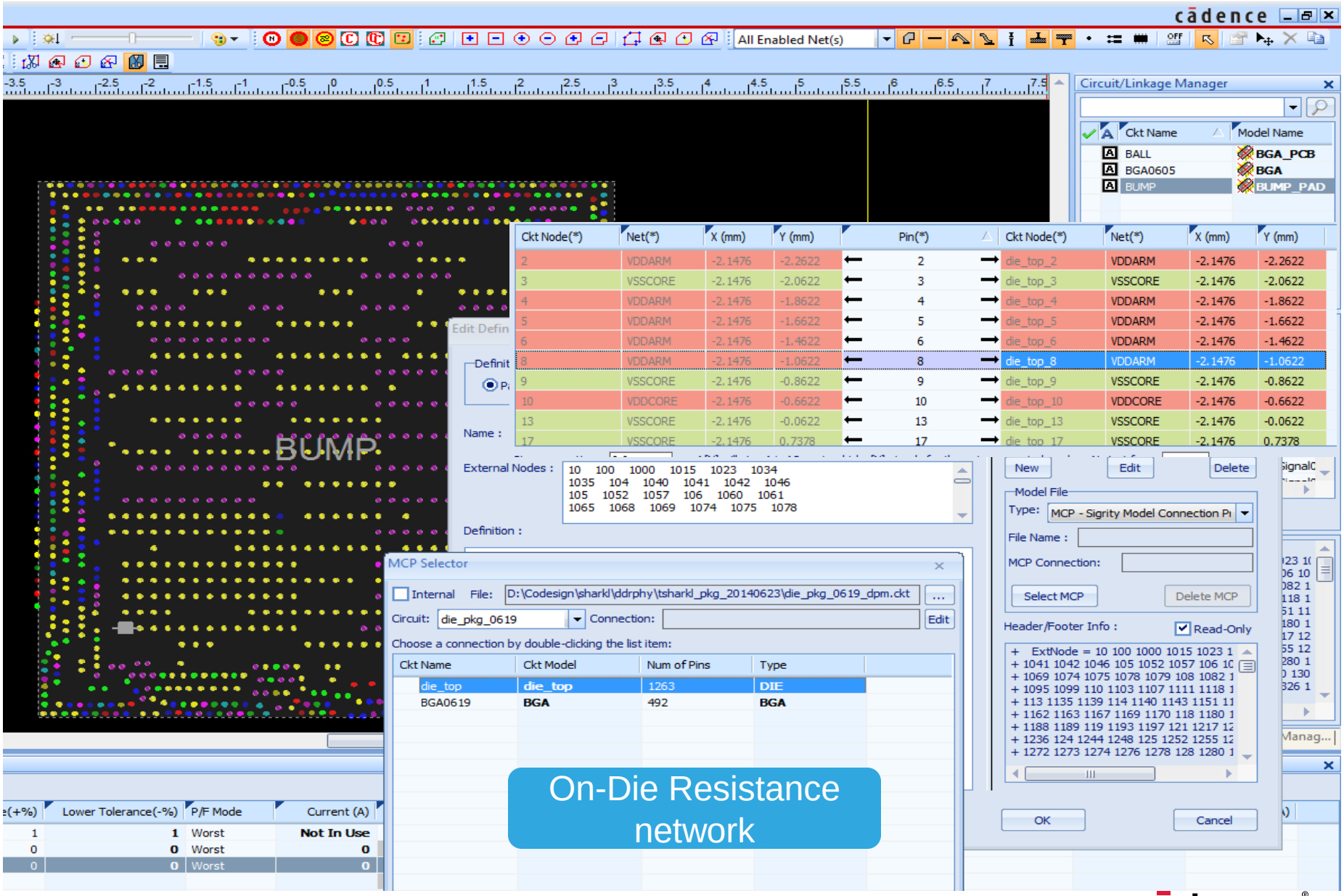


System-Centric DC IR-Drop simulation with DPM



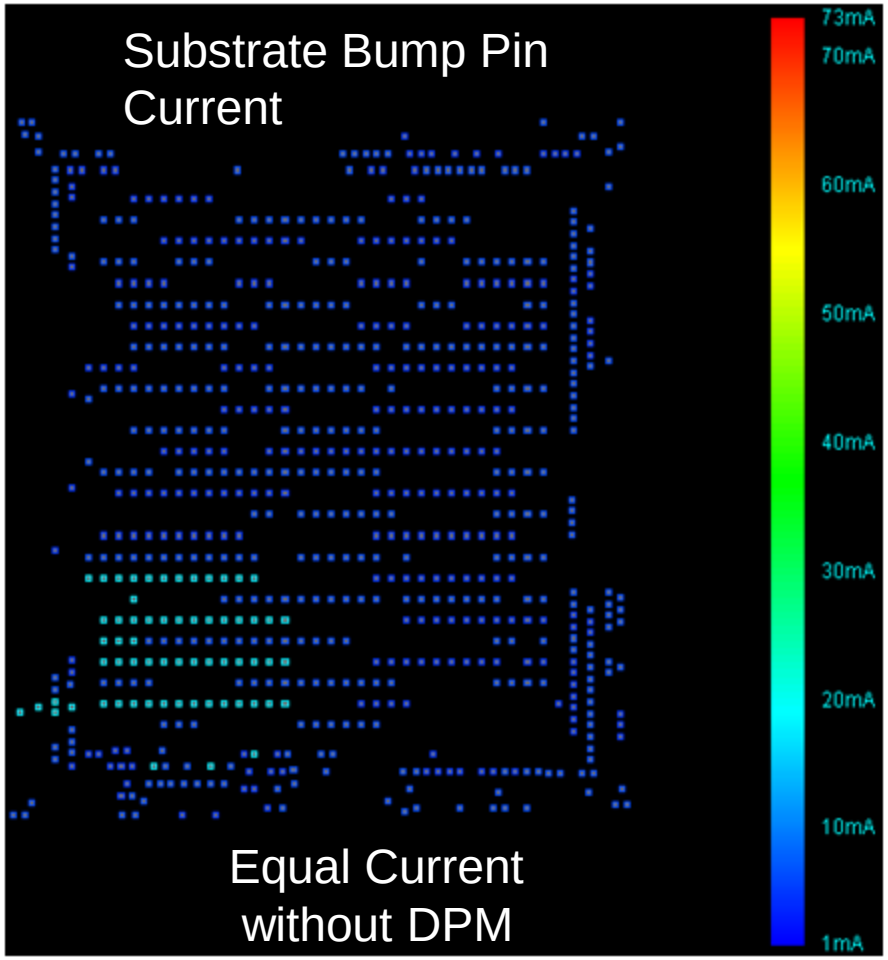
cadence

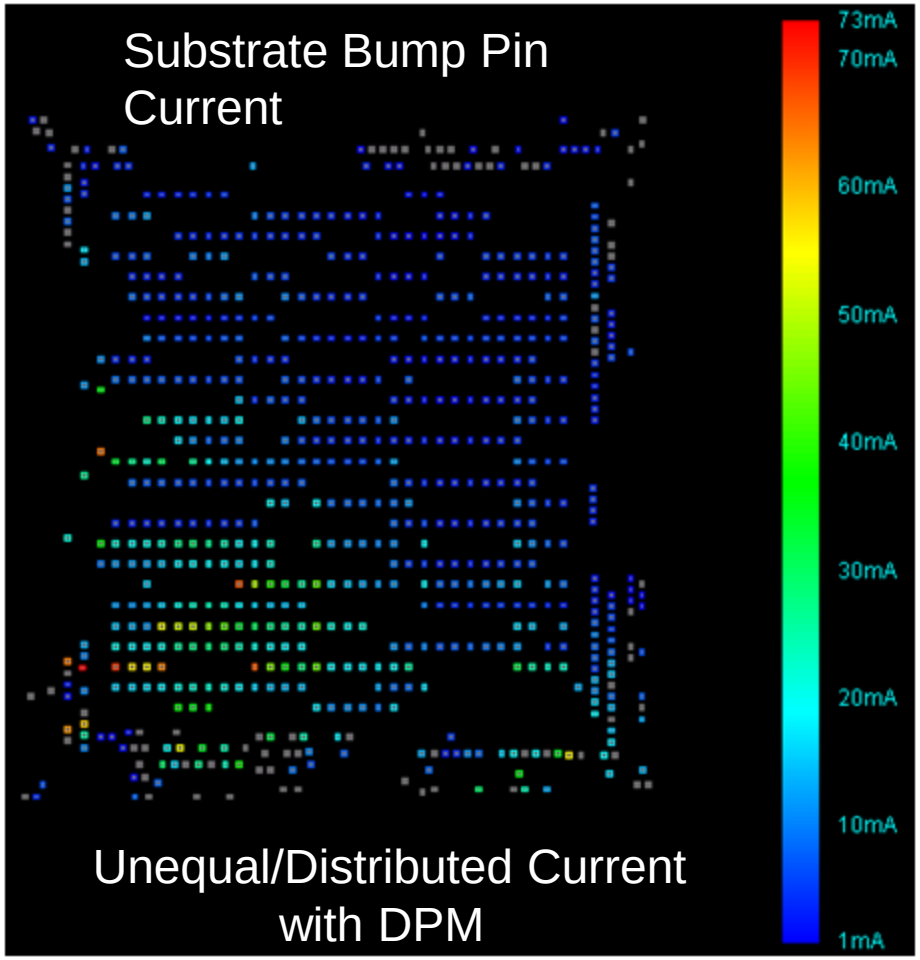
System-Centric DC IR-Drop simulation with DPM (cont.)



cadence

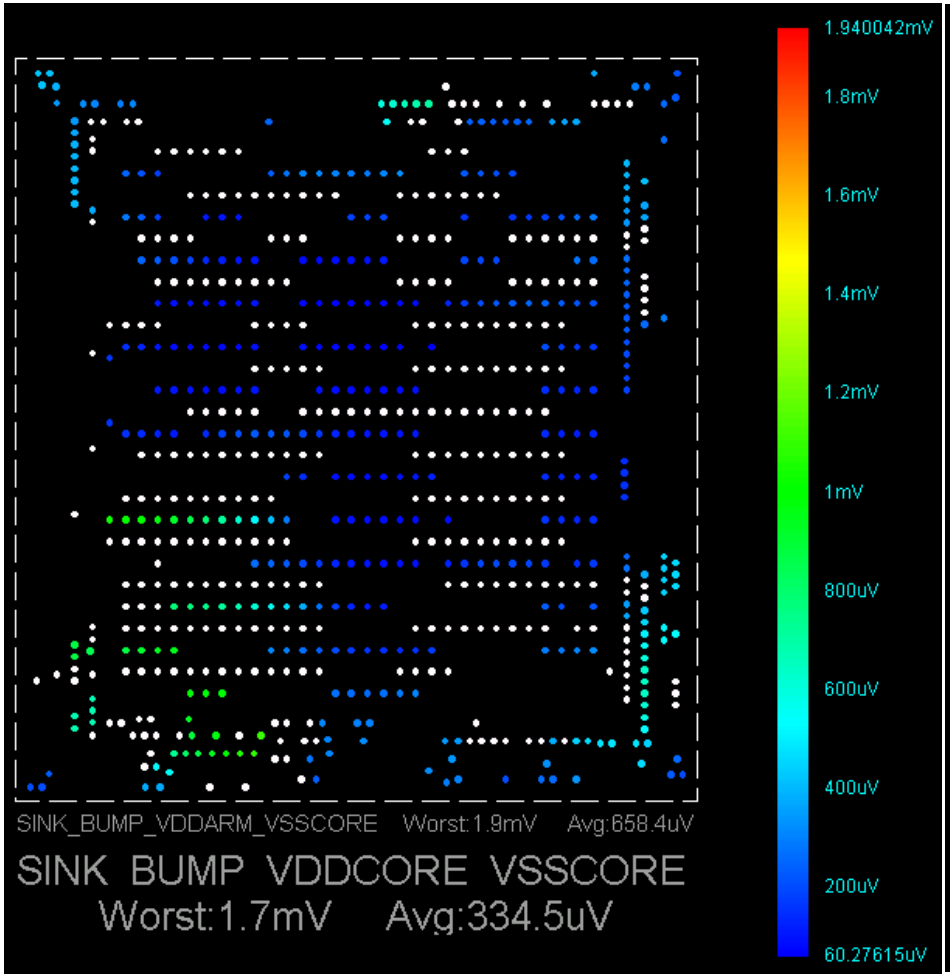
Package Bump Pad Current （without and with DPM）



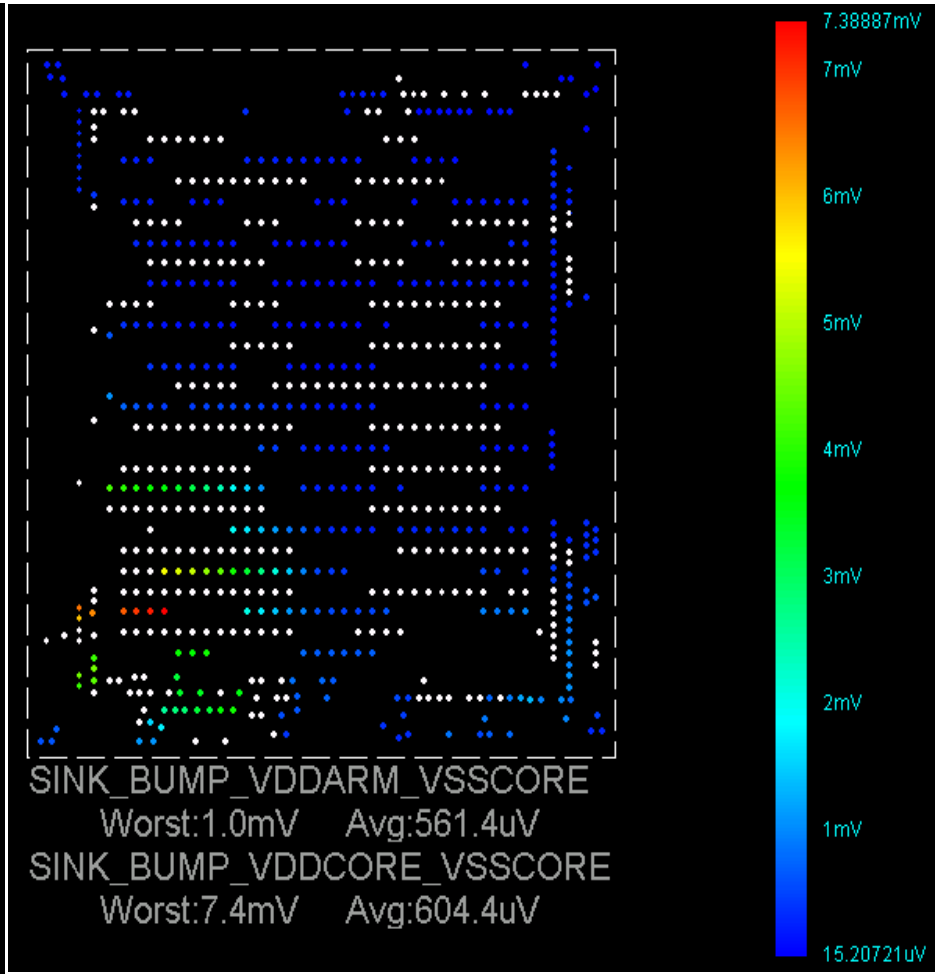


cadence

Package Bump Pad IR-Drop （without and with DPM）

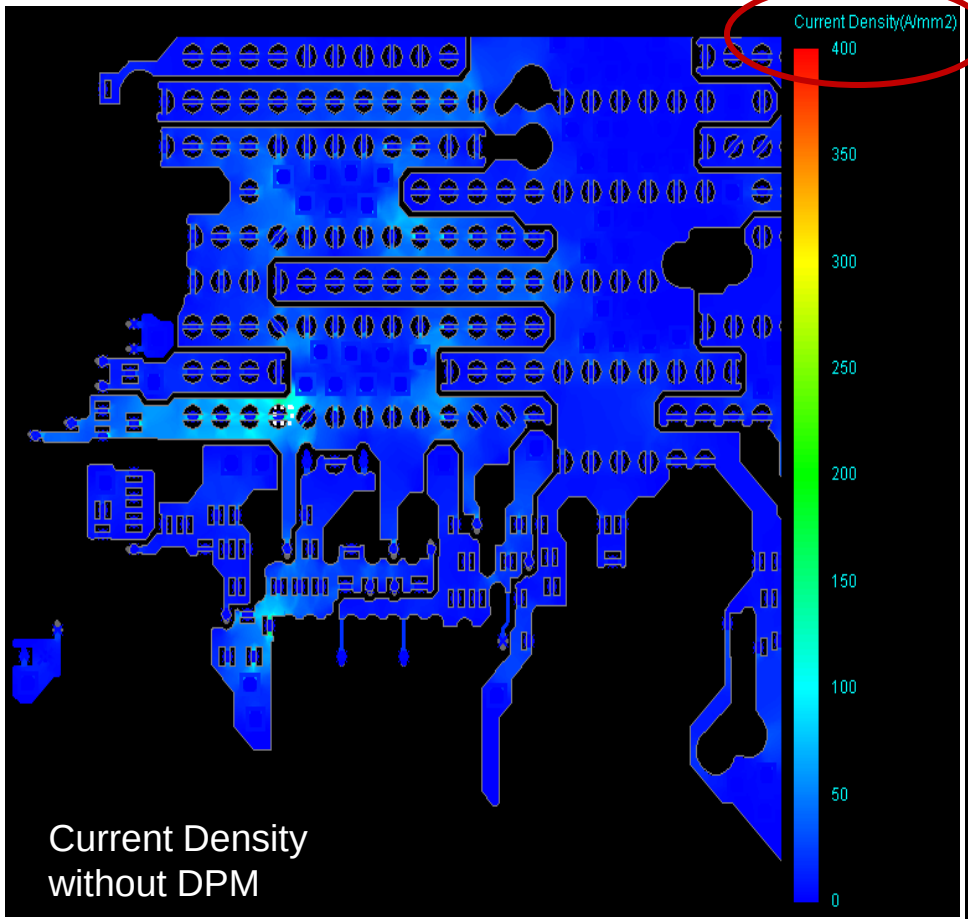


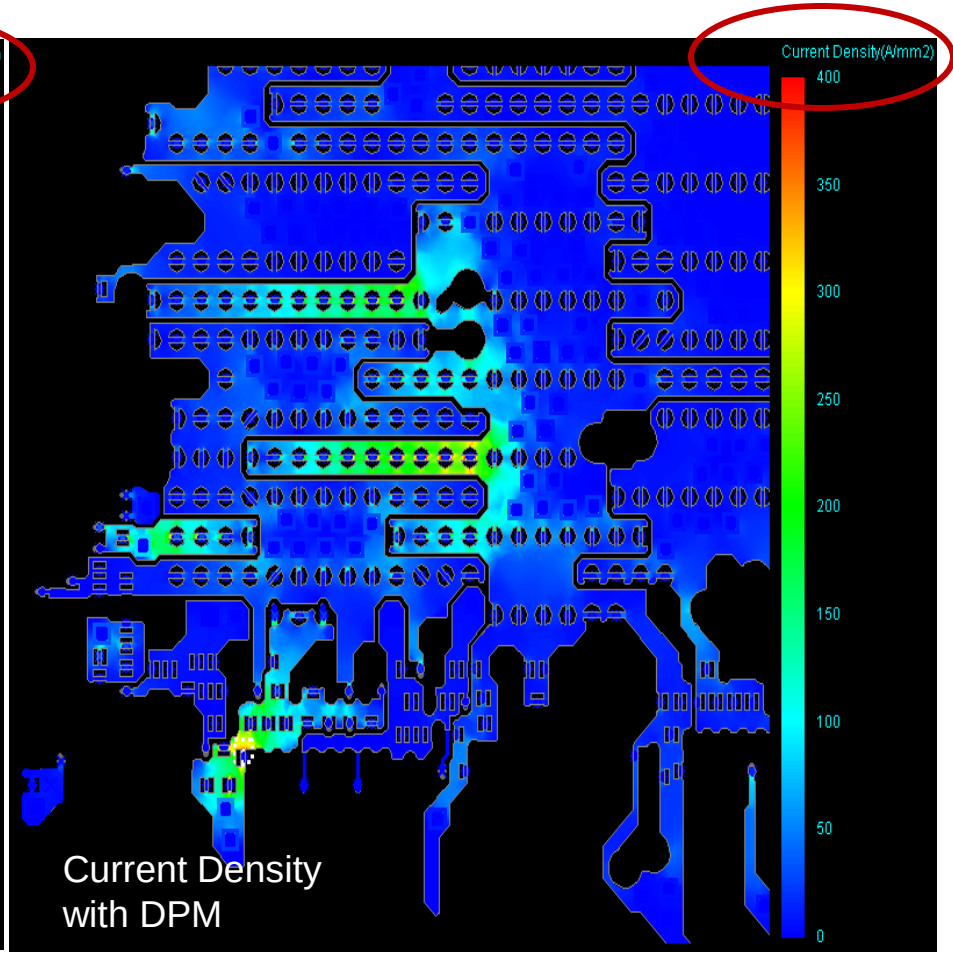
Equal Current without DPM



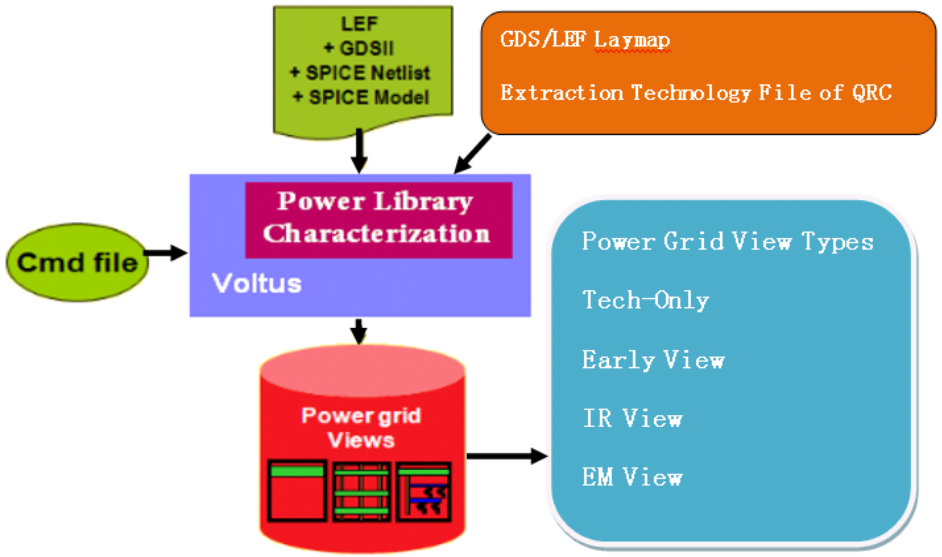
Unequal/Distributed Current with DPM

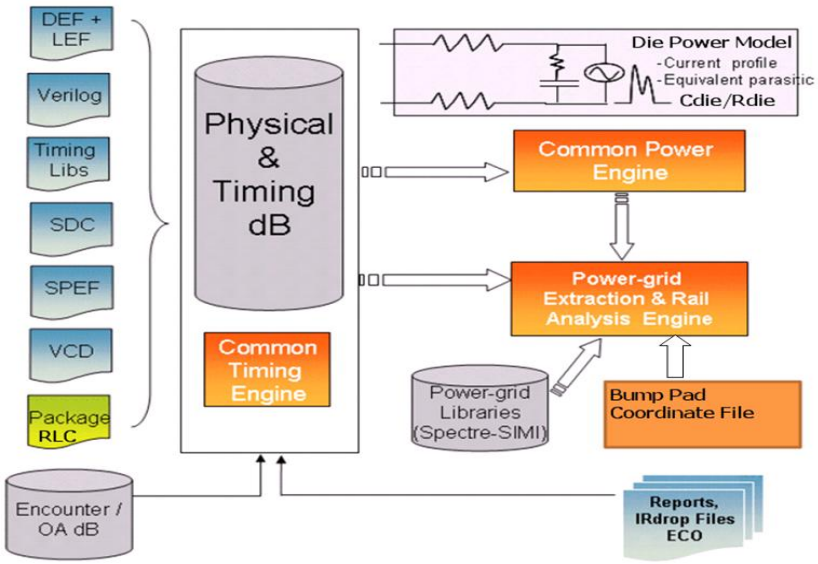
Package Current Density Distribution （without and with DPM）





Chip-centric Static/Dynamic IR-Drop Simulation





- set_package -spice ./via_pkg_dpm_0619_PinBaseSPICE.ckt
- set_rail_analysis_domain -name ALL -pwrnets VDDCORE -gndnets VSSCORE \
  -threshold 0.05

- set_power_pads -net VDDCORE -format xy -file VDDCORE.ppl.pkg
- set_power_pads -net VSSCORE -format xy -file VSSCORE.ppl.pkg

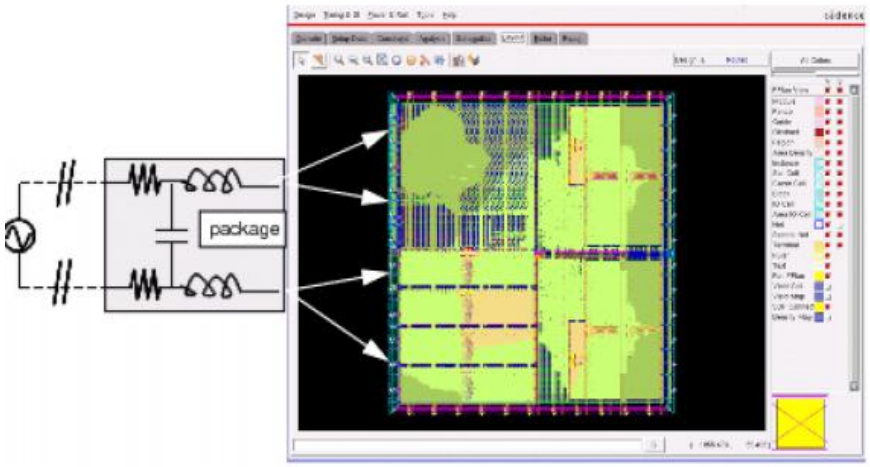
- analyze_rail -type domain -results_directory Dynamic_Result ALL

- create_die_model -model_transform_method res_shielding -state_directory Dynamic_Result/ALL_25C_dynamic_1 \
  -output_directory die_model -type n_port -rail_analysis_domain ALL

cadence

Link PPM Model with Voltus in IR-Drop Simulation

```
.SUBCKT die_pkg_0619
+              die_top_2            BGA0619_U11
+              die_top_4
+              die_top_5
```




```
*
*The following is the Cadence MCP(model connection protocol)
Section
************************************
*[MCP Begin]
*[MCP Ver] 1.1
*[Structure Type] PKG
*[MCP Source] Cadence Design Systems, Inc. XtractIM 13.0.2.05231
6/19/2014
*
************************************
*
*[REM]The following is the info for component connection die_top
*[REM]************************************
*[Connection] die_top die_top 1263
*[Connection Type] DIE
*[Power Nets]
*2    die_top_2  VDDARM     -0.0021476 -0.0022622
*4    die_top_4  VDDARM     -0.0021476 -0.0018622
*5    die_top_5  VDDARM     -0.0021476 -0.0016622
```

Total Distributed

```
Kd1_402 LD1 LD402 0.257499
Kd1_403 LD1 LD403 0.264899
Kd1_404 LD1 LD404 0.249644
Kd1_405 LD1 LD405 0.238175
Kd1_406 LD1 LD406 0.307995
Kd1_407 LD1 LD407 0.290569
Kd1_408 LD1 LD408 0.26358
R_11577 DrN156 DrN104 119.331
R_11578 DrN157 DrN104 101.849
R_11579 DrN158 DrN104 69860.7
R_11580 DrN159 DrN104 75352.9
R_11581 DrN160 DrN104 394599
R_11582 DrN161 DrN104 63596.1
R_11583 DrN162 DrN104 11613.6
```

```
LD66 die_top_18 DrN66 8.47554e-10
LD67 die_top_36 DrN67 3.09247e-10
LD68 die_top_38 DrN68 3.06801e-10
LD69 die_top_44 DrN69 8.27109e-10
LD70 die_top_48 DrN70 6.17681e-10
LD71 die_top_62 DrN71 2.81627e-10
LD72 die_top_64 DrN72 2.77682e-10
LD73 die_top_70 DrN73 8.56309e-10
LD74 die_top_72 DrN74 6.40649e-10
```

R L C K

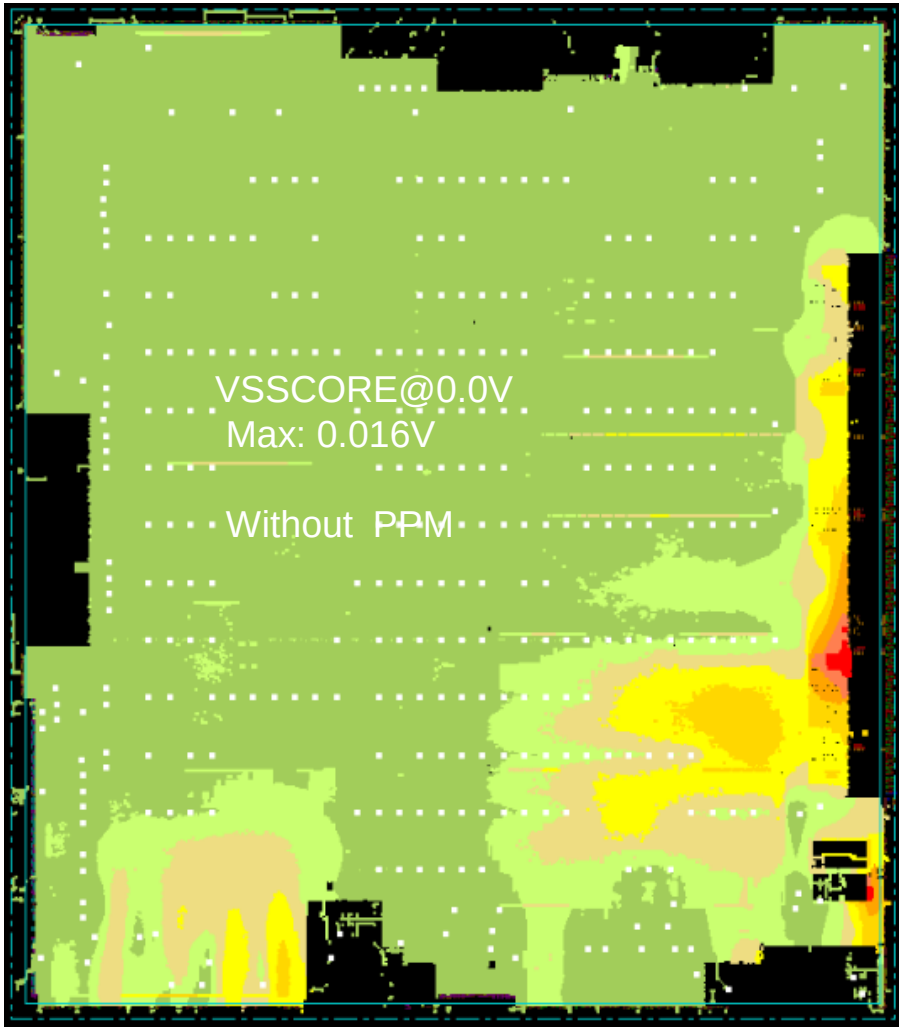
MCP

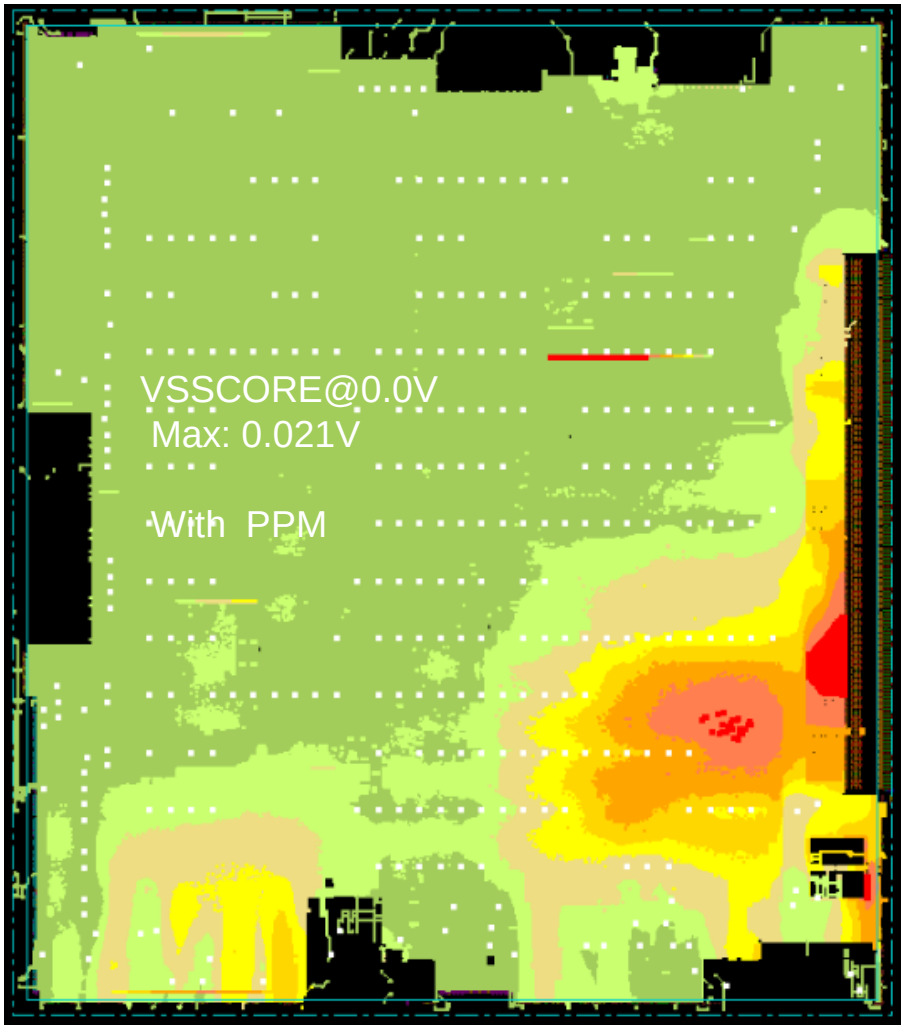
```
*[REM]The following is the info for component connection BGA0619
*[REM]************************************
*[Connection] BGA0619 BGA 492
*[Connection Type] BGA
*[Power Nets]
*U11  BGA0619_U11      VDDARM      -0.0016000 -0.0
*U12  BGA0619_U11      VDDARM      -0.0012000 -0.0
*U13  BGA0619_U11      VDDARM      -0.0008000 -0.0008000
*V11  BGA0619_U11      VDDARM      -0.0016000 -0.0012000
*V12  BGA0619_U11      VDDARM      -0.0012000 -0.0012000
*V13  BGA0619_U11      VDDARM      -0.0008000 -0.0012000
*W12  BGA0619_U11      VDDARM      -0.0012000 -0.0016000
*W13  BGA0619_U11      VDDARM      -0.0008000 -0.0016000
*W14  BGA0619_U11      VDDARM      -0.0004000 -0.0016000
*Y11  BGA0619_U11      VDDARM      -0.0016000 -0.0020000
*Y12  BGA0619_U11      VDDARM      -0.0012000 -0.0020000
*Y13  BGA0619_U11      VDDARM      -0.0008000 -0.0020000
*Y14  BGA0619_U11      VDDARM      -0.0004000 -0.0020000
*K13  BGA0619_K13      VDDCORE     -0.0008000 0.0020000
*K14  BGA0619_K13      VDDCORE     -0.0004000 0.0020000
*K15  BGA0619_K13      VDDCORE     0.0000000  0.0020000
*K16  BGA0619_K13      VDDCORE     0.0004000  0.0020000
*K17  BGA0619_K13      VDDCORE     0.0008000  0.0020000
*L16  BGA0619_K13      VDDCORE     0.0004000  0.0016000
*L17  BGA0619_K13      VDDCORE     0.0008000  0.0016000
*L18  BGA0619_K13      VDDCORE     0.0012000  0.0016000
```

Net Grouped

cadence

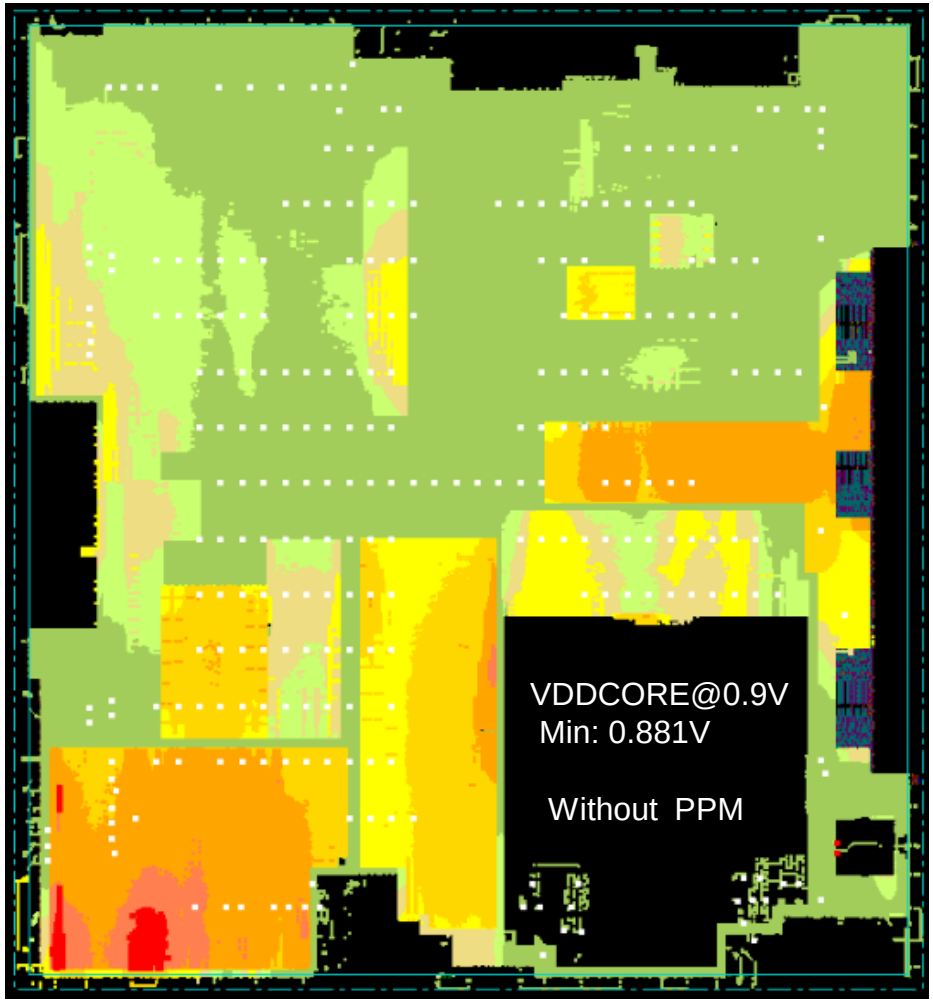
Chip VSSCORE Static IR-Drop （without and with PPM）

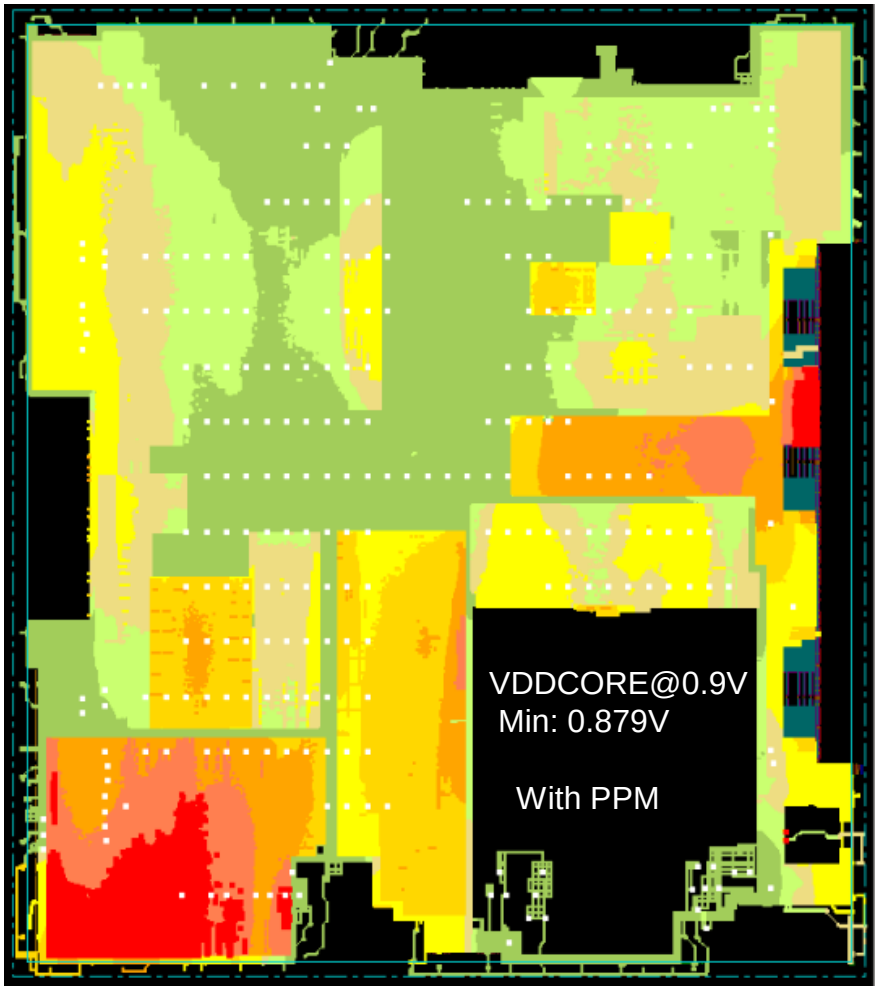




cadence

Chip VDDCORE Static IR-Drop （without and with PPM）





Summary

- The new Co-simulation methodology bridge cross domain (Package and IC) database interchange easily and effectively
- DPM model enables to predict more accurate current distribution on each bump pad, week design region and optimize the substrate design before chip tape
- Dynamic IR-Drop with PPM helps to find more real transient voltage and ripple noise, enable IC designer to optimize the on-chip Power Grid design

展讯通信®

SPREADTRUM®

cadence®

Thank You