

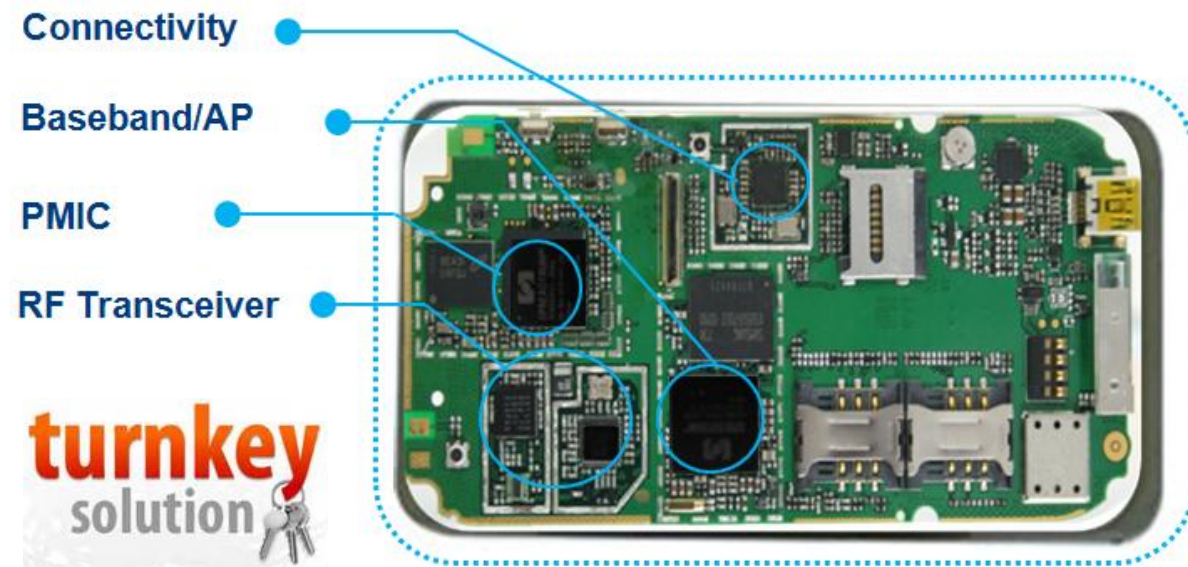
Holonomic Power Integrity Signoff Methodology of Mobile Baseband Processor

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IC-Packaging Codesign
Aug 5, 2014



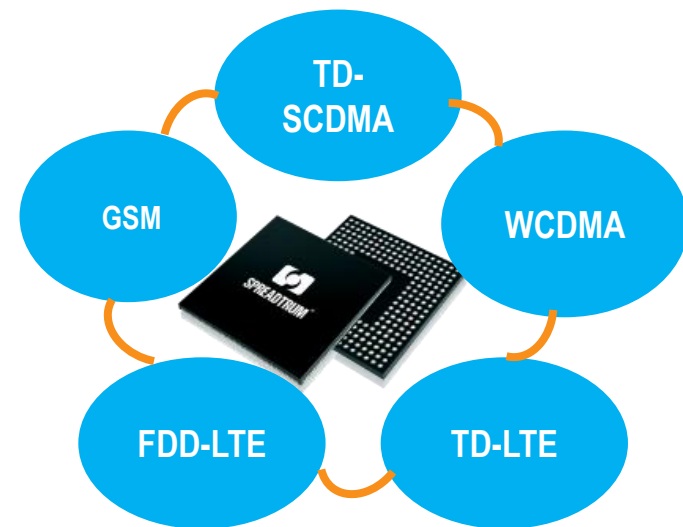
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Spreadtrum and Product Introduction



GSM/EDGE/TD-SCDMA/WCDMA/TD-LTE/FDD-LTE

Feature Phone /Smart Phone/Tablet / Datacard



Mobile Devices, Today & Tomorrow (I)

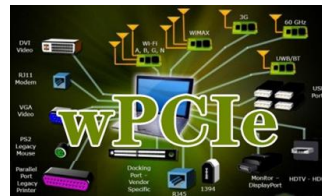
Lifelike
Graphics
Larger Display
Better User
Experience

High-Speed
Connectivity
3G/4G/5G

Smarter
Features

Biometrics/
Health/Medical

Computing
Everywhere
Multi-Core
Processing



Mobile Devices, Today & Tomorrow (II)

Higher graphic resolution
Heavier application

HD: 1280x720

2K: 1920x1080

4K: 3840x2160

8K: 7680x4320

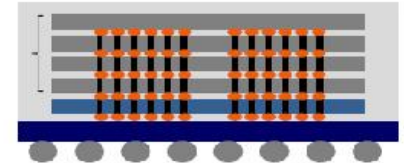


More density, higher band-width

LPDDR3 @2ch x32 x1600Mbps @12.8GBps

LPDDR4 @4ch x32 x3200Mbps @51.2GBps

Density: 16GB/24GB/32GB



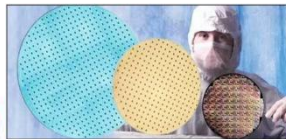
Technology

x64 @multi-GHz

Quad Core...

28nm/16nm/10nm

Less Power,
Always-on & Connected



18/12/8 inch
450/300/200mm

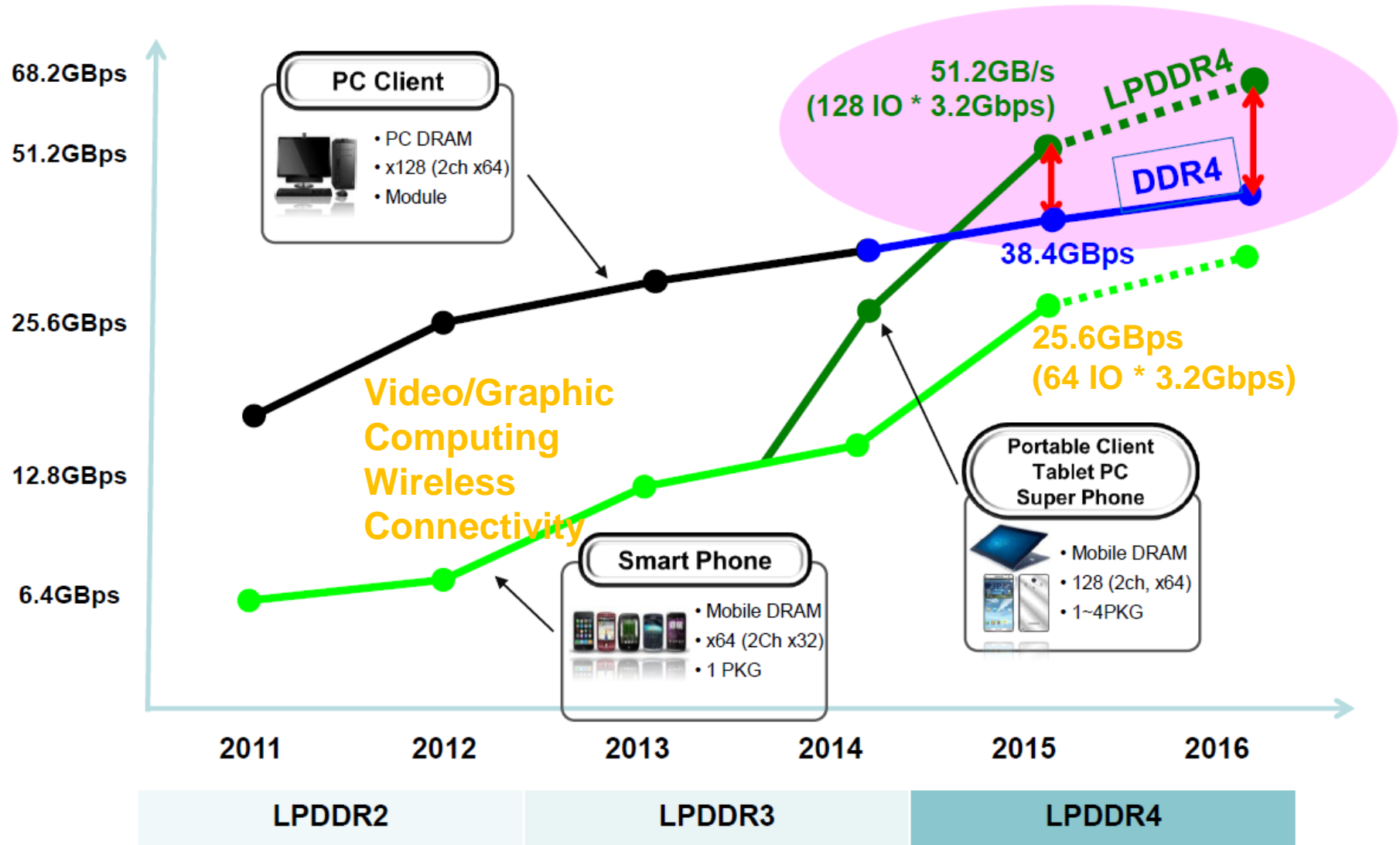
ALWAYS



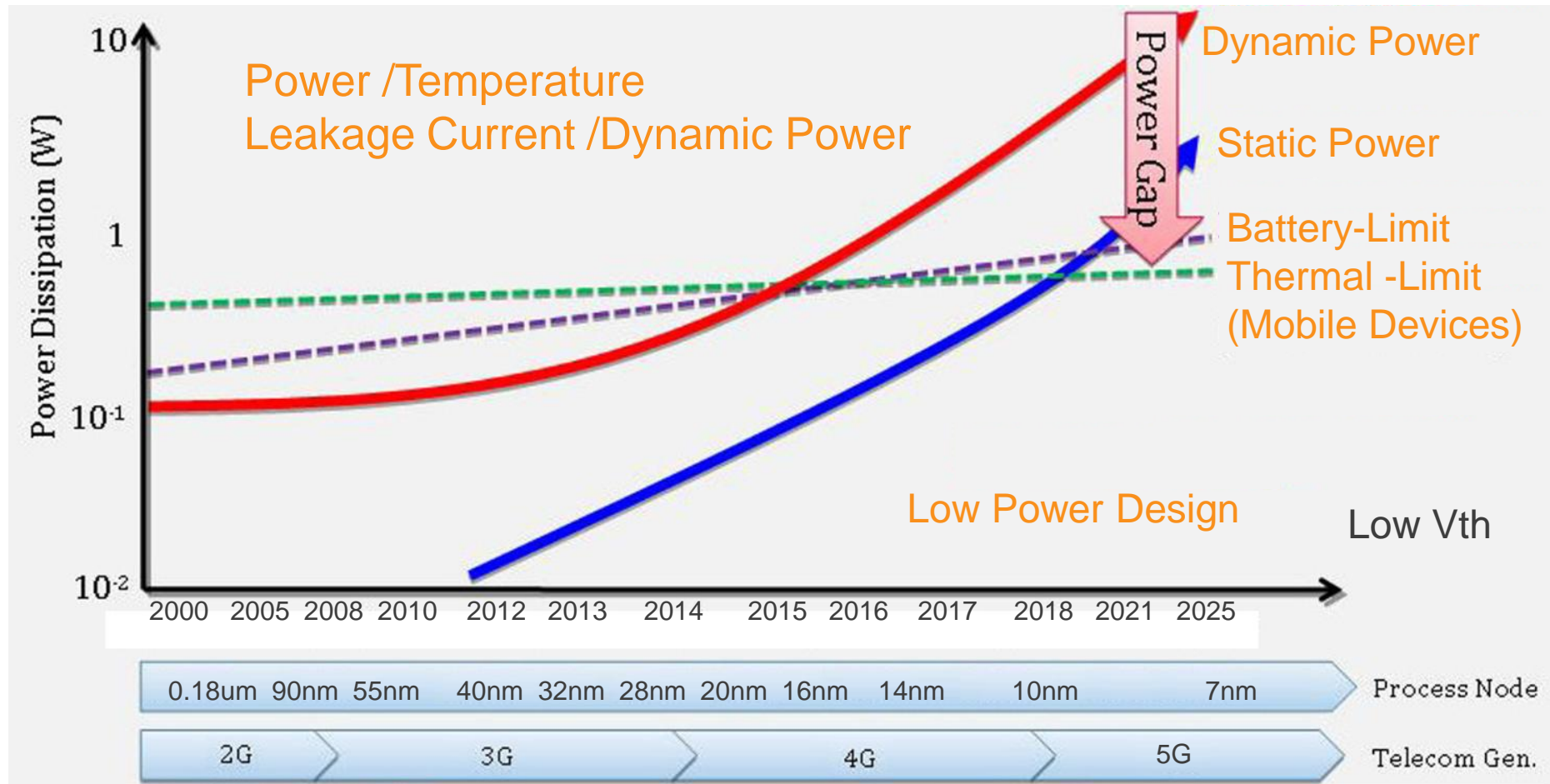
Thinner and Lighter



Mobile DRAM will Exceed PC DRAM Performance



Lower Power Design and Power Trend



Power Signoff Challenges of Mobile Chips

COST
DOWN

High
Performance

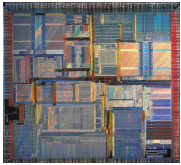
User Experience



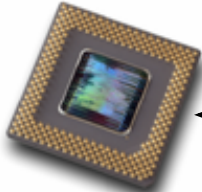
Less Design
Margin

VDD: 0.9V
 $L \cdot di/dt$
Lower V_t
Larger Leakage

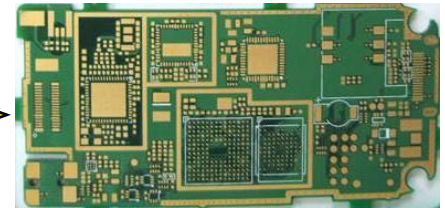
Power Integrity Analysis Collaborating Across Team



IC Power Analysis
Designer



Package Electrical
Analysis Engineer



System Electrical
Analysis Engineer

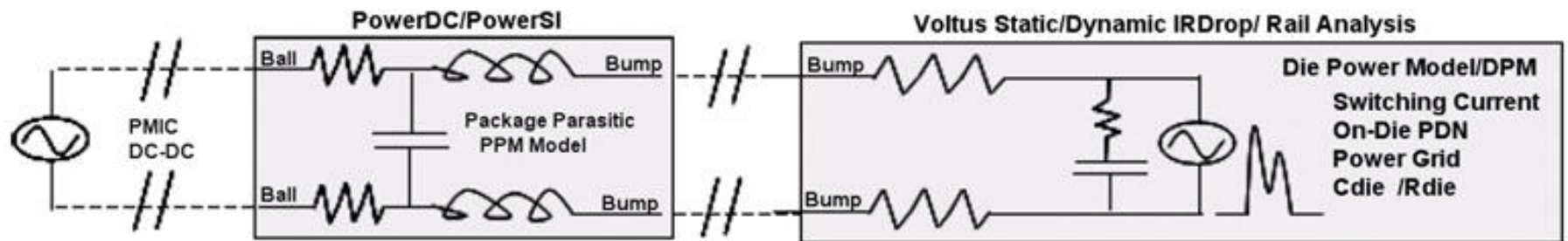
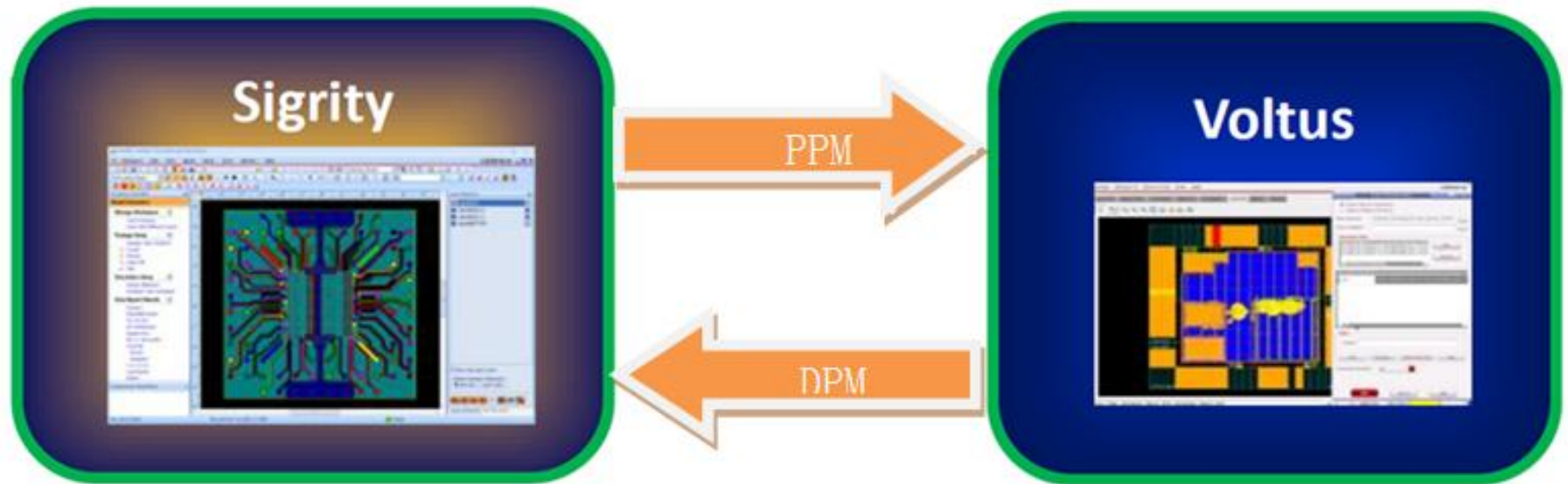
CoWork



PI is not just IC
Designer's Job

Designer's Job

System/IC-Centric PI Co-simulation

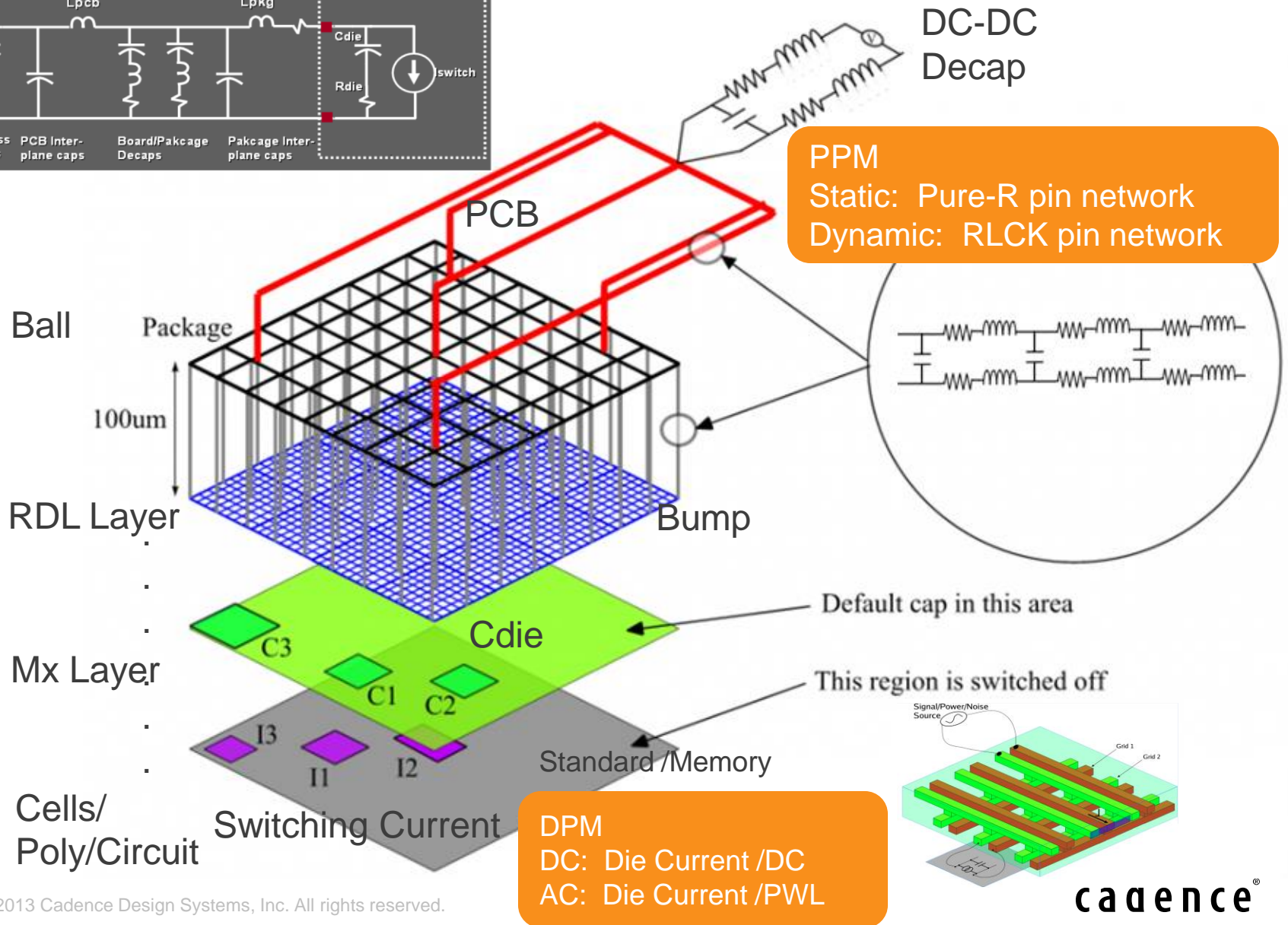
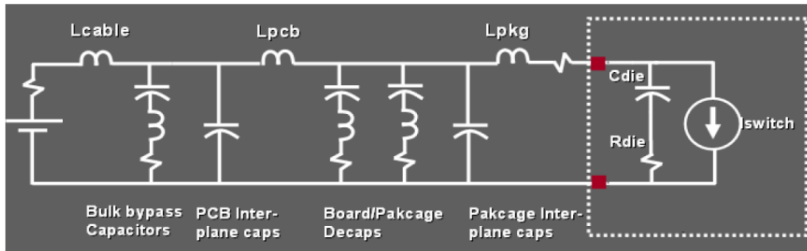


PMIC/DC-DC
PCB/Decap

On-Package IR-Drop
Source: Ball
Sink: Bump

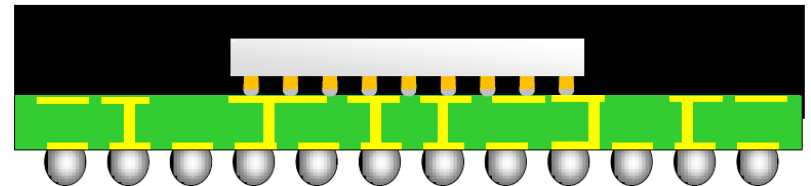
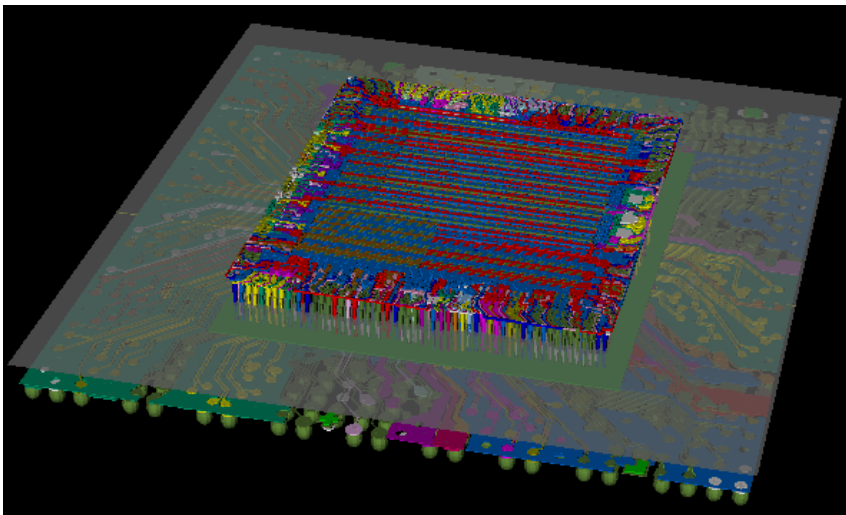
On-Chip IR-Drop
Source : Bump
Sink: Macros /Memory
Standard Cell

Schematic representation of a Chip/System Co-simulation



Flipchip Baseband /Application Processor Case

- Ball: 492
- Bumps: 1537
- Power Net: VDDCORE 0.9V (TT)
- VDDARM 1.0V (TT)
- Ground Net: VSSCORE



System-Centric DC IR-Drop simulation with DPM

The screenshot displays the Cadence PowerDC software interface for IR Drop Analysis. The left sidebar shows the workflow steps: IR Drop Analysis, Resistance Measurement, Generate Resistance Network Model, Advanced Thermal, and Pin Location Effectiveness. The 'Initial Setup' section includes options like 'Load a New/Different Layout', 'Check Stackup', 'Via Plating Thickness Setup', 'Select Pwr/Gnd Nets', and 'Include Thermal Effect'. The 'Voltage Drop Analysis Setup' section is active, showing 'Setup VRMs', 'Setup Sinks', 'Setup Interconnects', and 'Other'. The 'Constraints Setup' and 'Simulate' sections are also visible.

The main workspace shows a grid of nodes representing the power distribution network. A yellow arrow points from the 'Current Mapping File' section to the 'Current (A)' column in the results table.

Current Mapping File

Node Name	Net	Current (A)	Total Current
Node021008!! 160::...	VDDARM	0.0280833	
Node021010!! 162::...	VDDARM	0.0243867	
Node021011!! 164::...	VDDARM	0.0193067	
Node021025!! 184::...	VDDARM	0.0217267	
Node021026!! 186::...	VDDARM	0.0282467	
Node021028!! 188::...	VDDARM	0.0233433	
Node021029!! 190::...	VDDARM	0.0192967	

Voltage Drop Analysis Setup -> Setup Sinks

Sink Name	Model	Nominal Voltage (V)	Power/Ground Net	Upper Tolerance(+%)	Lower Tolerance(-%)	P/F Mode	Current (A)	Current Mapping File
SINK_BUMP_VDDARM	Unequal Current	0.9	VDDARM_VSSCORE	1	1	Worst	Not In Use	
SINK_BUMP_VDDCORE	Equal Voltage Equal Current Unequal Current	0.9	VDDCORE_VSSCORE	1	1	Worst	Not In Use	

System-Centric DC IR-Drop simulation with DPM (cont.)

The screenshot displays the Cadence Allegro DPM interface for a system-centric DC IR-drop simulation. The main workspace shows a die layout with a central bump area labeled "BUMP". Overlaid on this are several windows:

- Circuit/Linkage Manager:** A table listing components and their models.

Ckt Name	Model Name
BALL	BGA_PCB
BGA0605	BGA
BUMP	BUMP_PAD
- Pin Connection Table:** A table showing connections between die pins and top pins.

Ckt Node(*)	Net(*)	X (mm)	Y (mm)	Pin(*)	Ckt Node(*)	Net(*)	X (mm)	Y (mm)
2	VDDARM	-2.1476	-2.2622	2	die_top_2	VDDARM	-2.1476	-2.2622
3	VSSCORE	-2.1476	-2.0622	3	die_top_3	VSSCORE	-2.1476	-2.0622
4	VDDARM	-2.1476	-1.8622	4	die_top_4	VDDARM	-2.1476	-1.8622
5	VDDARM	-2.1476	-1.6622	5	die_top_5	VDDARM	-2.1476	-1.6622
6	VDDARM	-2.1476	-1.4622	6	die_top_6	VDDARM	-2.1476	-1.4622
8	VDDARM	-2.1476	-1.0622	8	die_top_8	VDDARM	-2.1476	-1.0622
9	VSSCORE	-2.1476	-0.8622	9	die_top_9	VSSCORE	-2.1476	-0.8622
10	VDDCORE	-2.1476	-0.6622	10	die_top_10	VDDCORE	-2.1476	-0.6622
13	VSSCORE	-2.1476	-0.0622	13	die_top_13	VSSCORE	-2.1476	-0.0622
17	VSSCORE	-2.1476	0.7378	17	die_top_17	VSSCORE	-2.1476	0.7378
- MCP Selector:** A window for selecting a connection. It shows a list of external nodes and a table of connections.

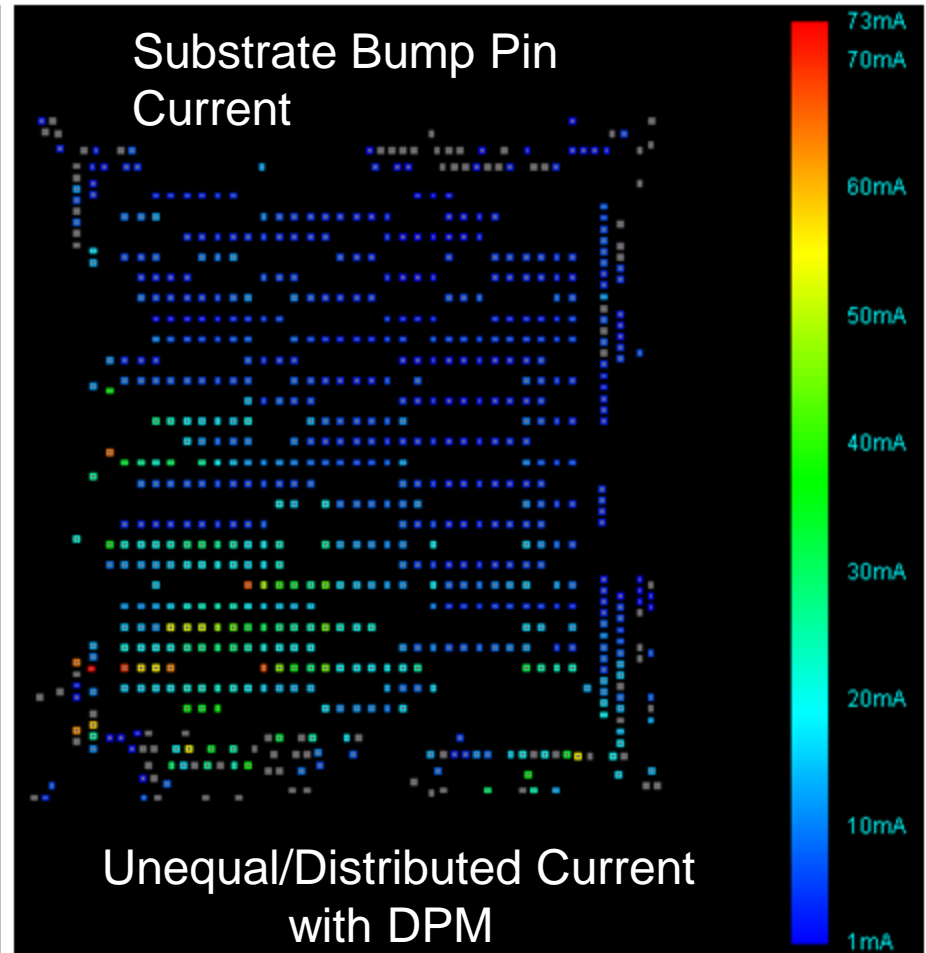
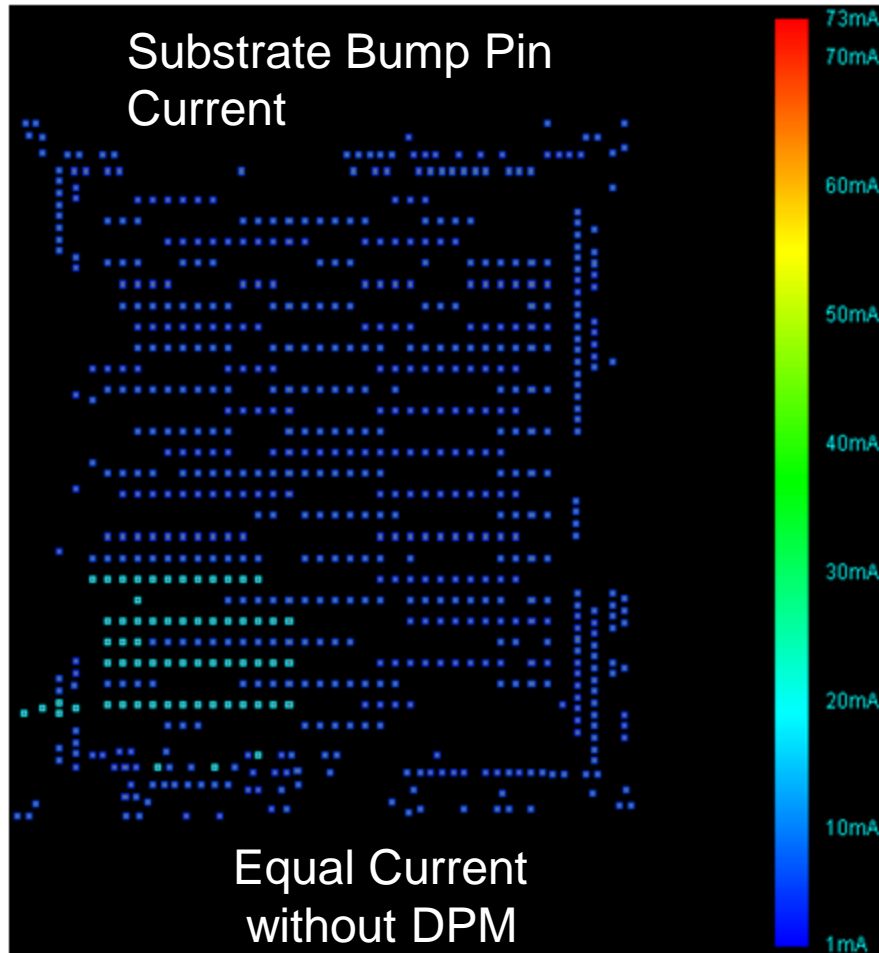
Ckt Name	Ckt Model	Num of Pins	Type
die_top	die_top	1263	DIE
BGA0619	BGA	492	BGA
- Header/Footer Info:** A window showing a list of external nodes and their connections.


```

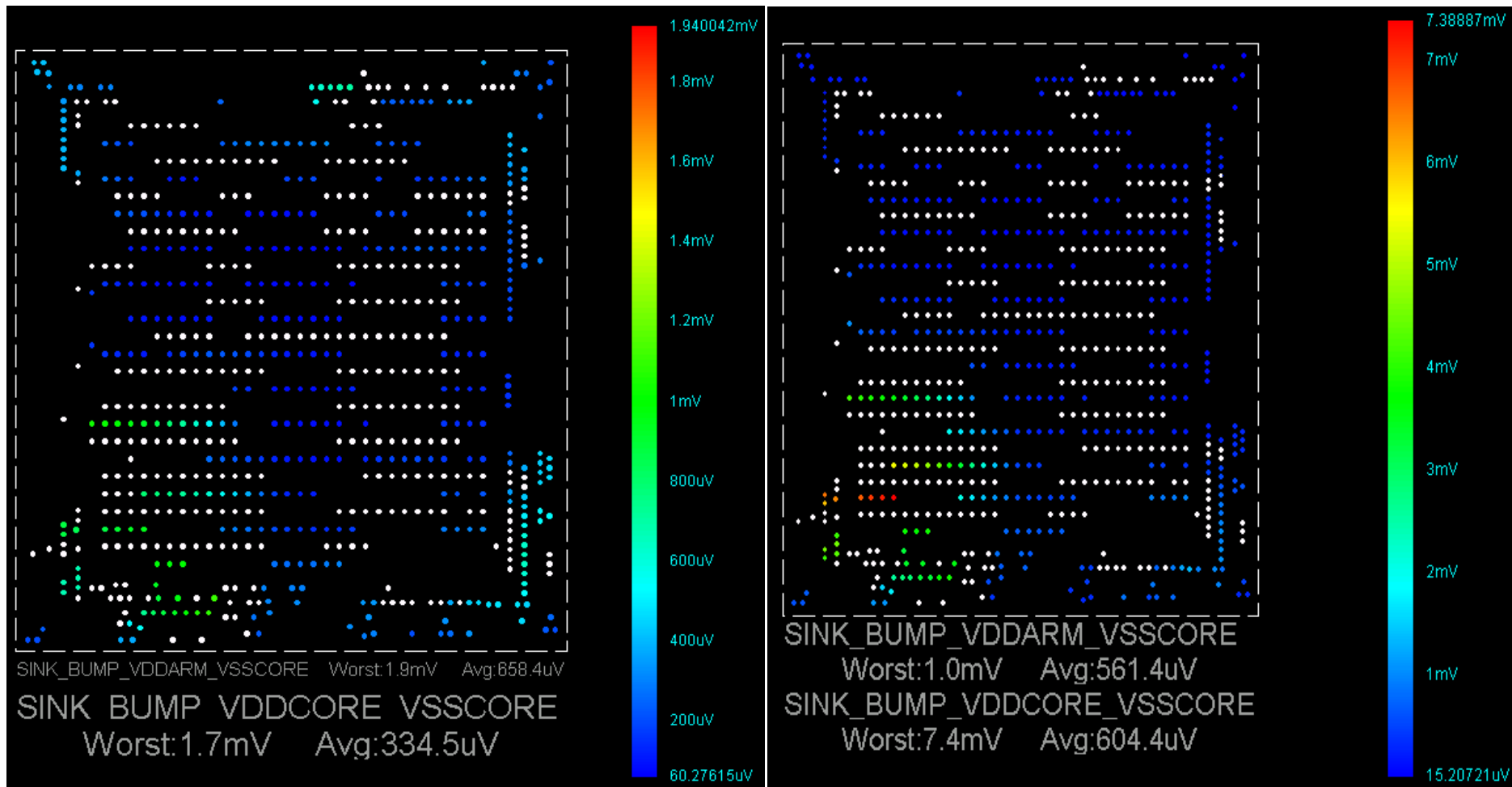
+ ExtNode = 10 100 1000 1015 1023 1034
+ 1041 1042 1046 105 1052 1057 106 10
+ 1069 1074 1075 1078 1079 108 1082 1
+ 1095 1099 110 1103 1107 1111 1118 1
+ 113 1135 1139 114 1140 1143 1151 11
+ 1162 1163 1167 1169 1170 118 1180 1
+ 1188 1189 119 1193 1197 121 1217 12
+ 1236 124 1244 1248 125 1252 1255 12
+ 1272 1273 1274 1276 1278 128 1280 1
      
```

A blue callout box at the bottom center reads "On-Die Resistance network".

Package Bump Pad Current (without and with DPM)



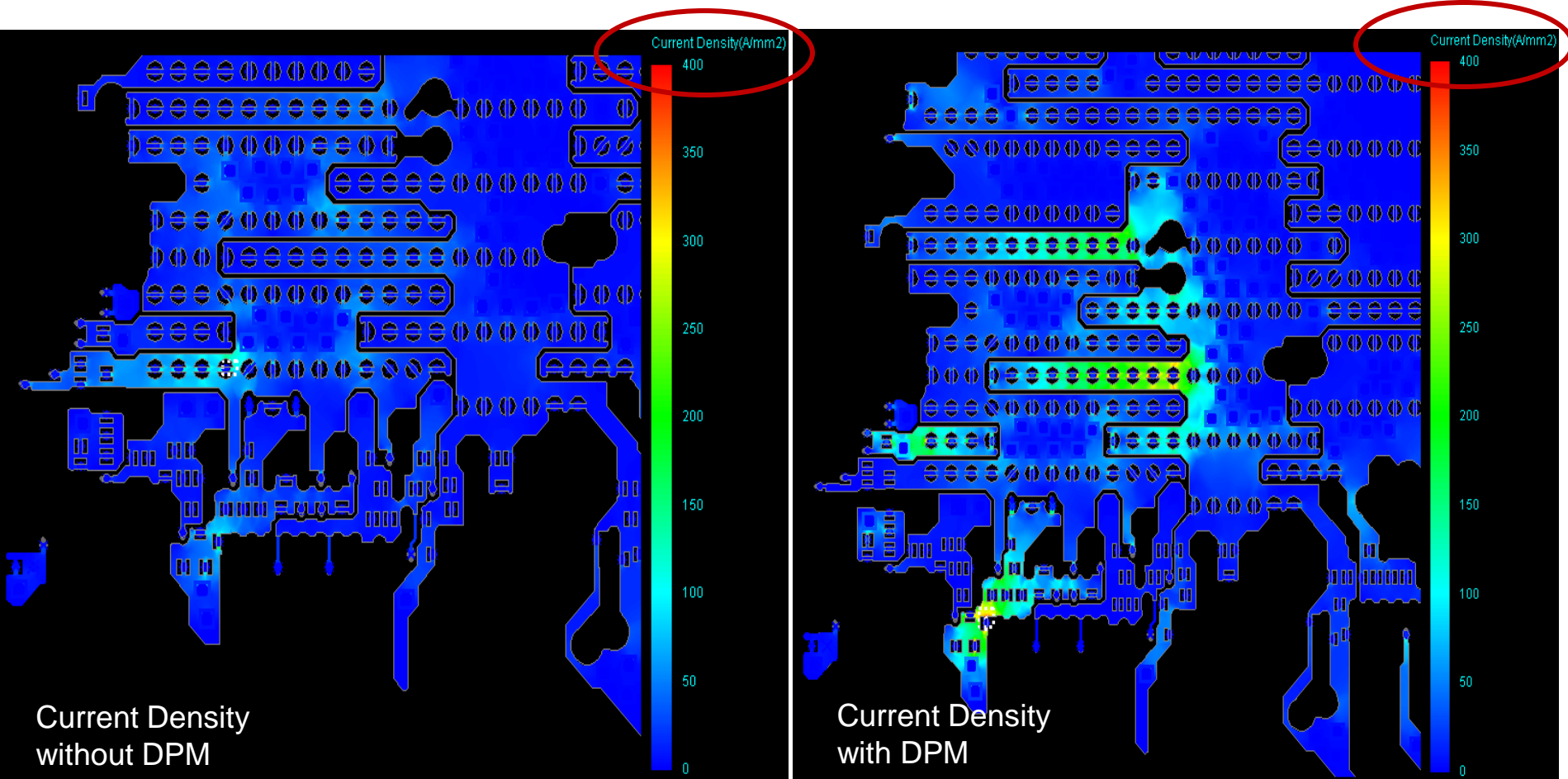
Package Bump Pad IR-Drop (without and with DPM)



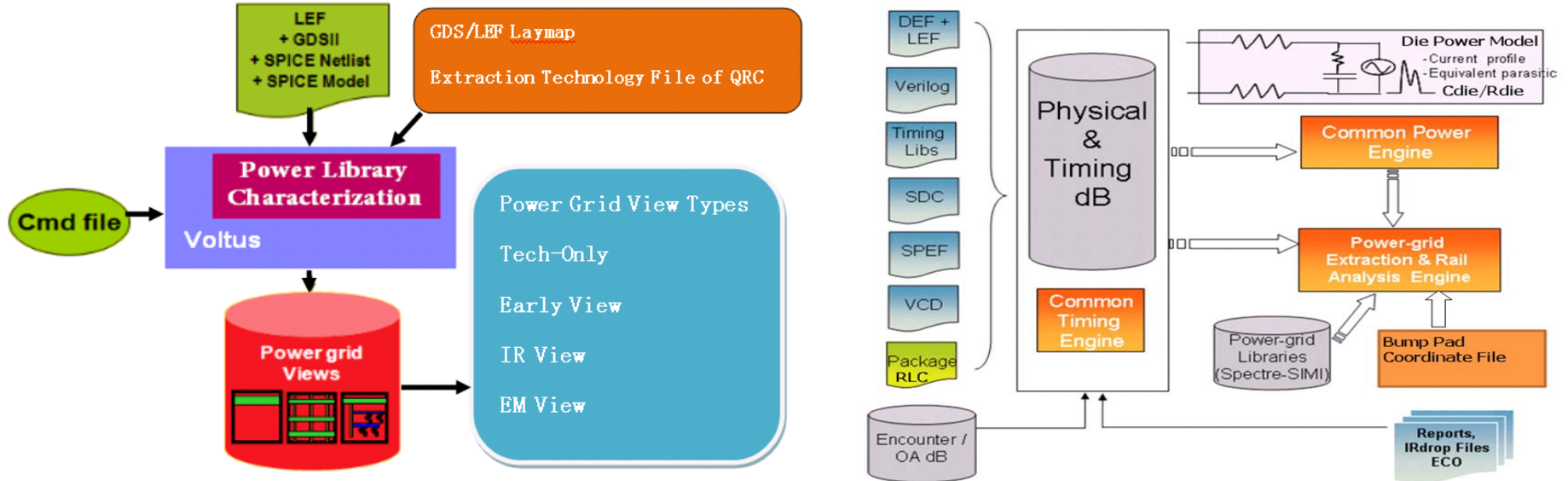
Equal Current without DPM

Unequal/Distributed Current with DPM

Package Current Density Distribution (without and with DPM)



Chip-centric Static/Dynamic IR-Drop Simulation



```

- set_package-spice ./via_pkg_dpm_0619_PinBaseSPICE.ckt
- set_rail_analysis_domain -name ALL -pwrnets VDDCORE -gndnets VSSCORE \
  -threshold 0.05

```

```

- set_power_pads -net VDDCORE -format xy -file VDDCORE.ppl.pkg
- set_power_pads -net VSSCORE -format xy -file VSSCORE.ppl.pkg

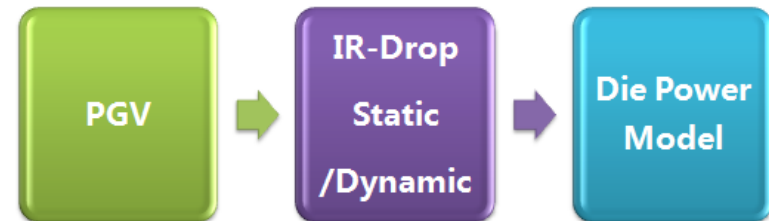
- analyze_rail -type domain -results_directory Dynamic_Result ALL

```

```

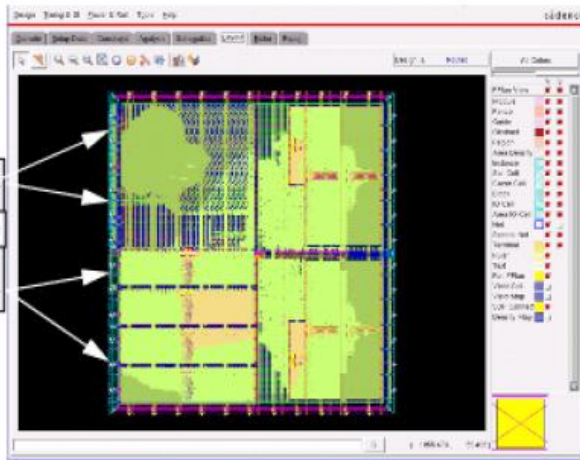
- create_die_model -model_transform_method res_shielding -state_directory
  Dynamic_Result/ALL_25C_dynamic_1\
  -output_directory die_model -type n_port -rail_analysis_domain ALL

```



Link PPM Model with Voltus in IR-Drop Simulation

```
.SUBCKT die_pkg_0619
+       die_top_2          BGA0619_U11
+       die_top_4
+       die_top_5
```



```
Kd1_402 LD1 LD402 0.257499
Kd1_403 LD1 LD403 0.264899
Kd1_404 LD1 LD404 0.249644
Kd1_405 LD1 LD405 0.238175
Kd1_406 LD1 LD406 0.307995
Kd1_407 LD1 LD407 0.290569
Kd1_408 LD1 LD408 0.26358
R_11577 DrN156 DrN104 119.331
R_11578 DrN157 DrN104 101.849
R_11579 DrN158 DrN104 69860.7
R_11580 DrN159 DrN104 75352.9
R_11581 DrN160 DrN104 394599
R_11582 DrN161 DrN104 63596.1
R_11583 DrN162 DrN104 11613.6
```

```
LD66 die_top_18 DrN66 8.47554e-10
LD67 die_top_36 DrN67 3.09247e-10
LD68 die_top_38 DrN68 3.06801e-10
LD69 die_top_44 DrN69 8.27109e-10
LD70 die_top_48 DrN70 6.17681e-10
LD71 die_top_62 DrN71 2.81627e-10
LD72 die_top_64 DrN72 2.77682e-10
LD73 die_top_70 DrN73 8.56309e-10
LD74 die_top_72 DrN74 6.40649e-10
```

R L C K
MCP

*[REM]The following is the info for component connection BGA0619

*[REM]*****

*[Connection] BGA0619 BGA 492

*[Connection Type] BGA

*[Power Nets]

*U11	BGA0619_U11	VDDARM	-0.001600	-0.001600
*U12	BGA0619_U11	VDDARM	-0.0012000	-0.0012000
*U13	BGA0619_U11	VDDARM	-0.0008000	-0.0008000
*V11	BGA0619_U11	VDDARM	-0.0016000	-0.0012000
*V12	BGA0619_U11	VDDARM	-0.0012000	-0.0012000
*V13	BGA0619_U11	VDDARM	-0.0008000	-0.0012000
*W12	BGA0619_U11	VDDARM	-0.0012000	-0.0016000
*W13	BGA0619_U11	VDDARM	-0.0008000	-0.0016000
*W14	BGA0619_U11	VDDARM	-0.0004000	-0.0016000
*Y11	BGA0619_U11	VDDARM	-0.0016000	-0.0020000
*Y12	BGA0619_U11	VDDARM	-0.0012000	-0.0020000
*Y13	BGA0619_U11	VDDARM	-0.0008000	-0.0020000
*Y14	BGA0619_U11	VDDARM	-0.0004000	-0.0020000
*K13	BGA0619_K13	VDDCORE	-0.0008000	0.0020000
*K14	BGA0619_K13	VDDCORE	-0.0004000	0.0020000
*K15	BGA0619_K13	VDDCORE	0.0000000	0.0020000
*K16	BGA0619_K13	VDDCORE	0.0004000	0.0020000
*K17	BGA0619_K13	VDDCORE	0.0008000	0.0020000
*L16	BGA0619_K13	VDDCORE	0.0004000	0.0016000
*L17	BGA0619_K13	VDDCORE	0.0008000	0.0016000
*L18	BGA0619_K13	VDDCORE	0.0012000	0.0016000

**Net
Grouped**

```
*
*The following is the Cadence MCP(model connection protocol)
Section
*****
*[MCP Begin]
*[MCP Ver] 1.1
*[Structure Type] PKG
*[MCP Source] Cadence Design Systems, Inc. XtractIM 13.0.2.05231
6/19/2014
*****
```

*[REM]The following is the info for component connection die_top

*[REM]*****

*[Connection] die_top die_top 1263

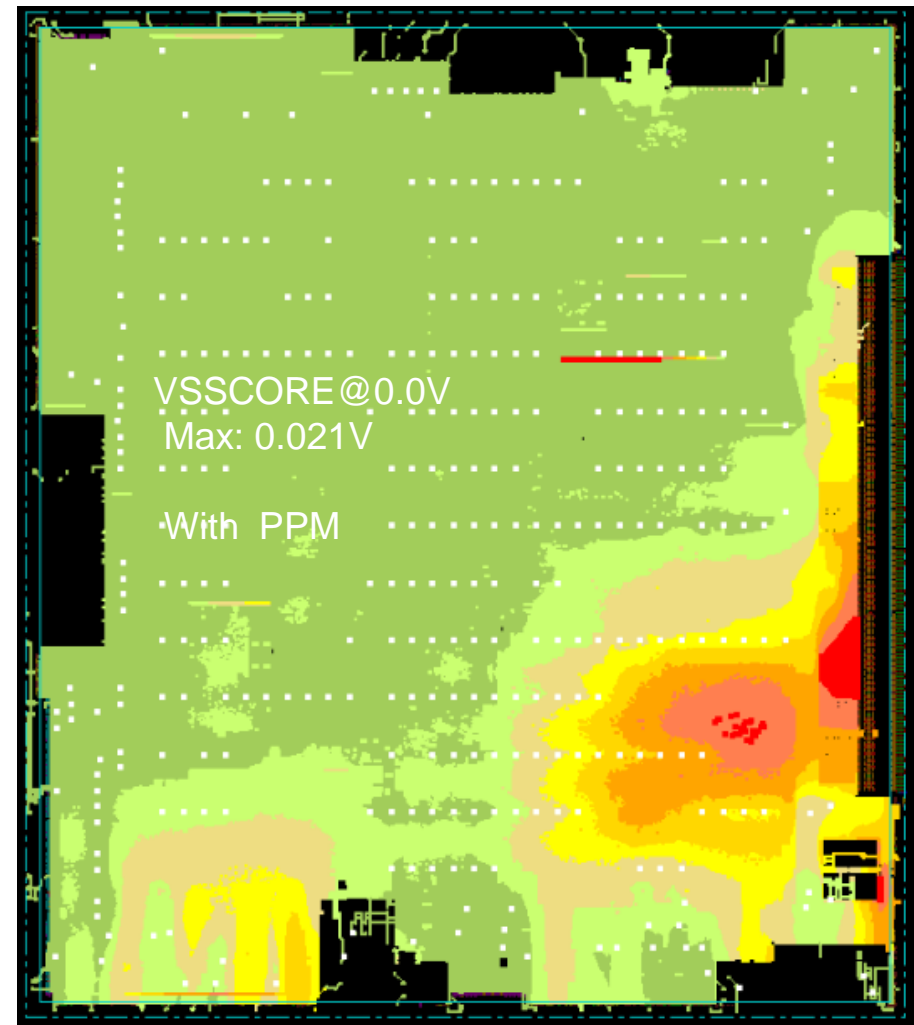
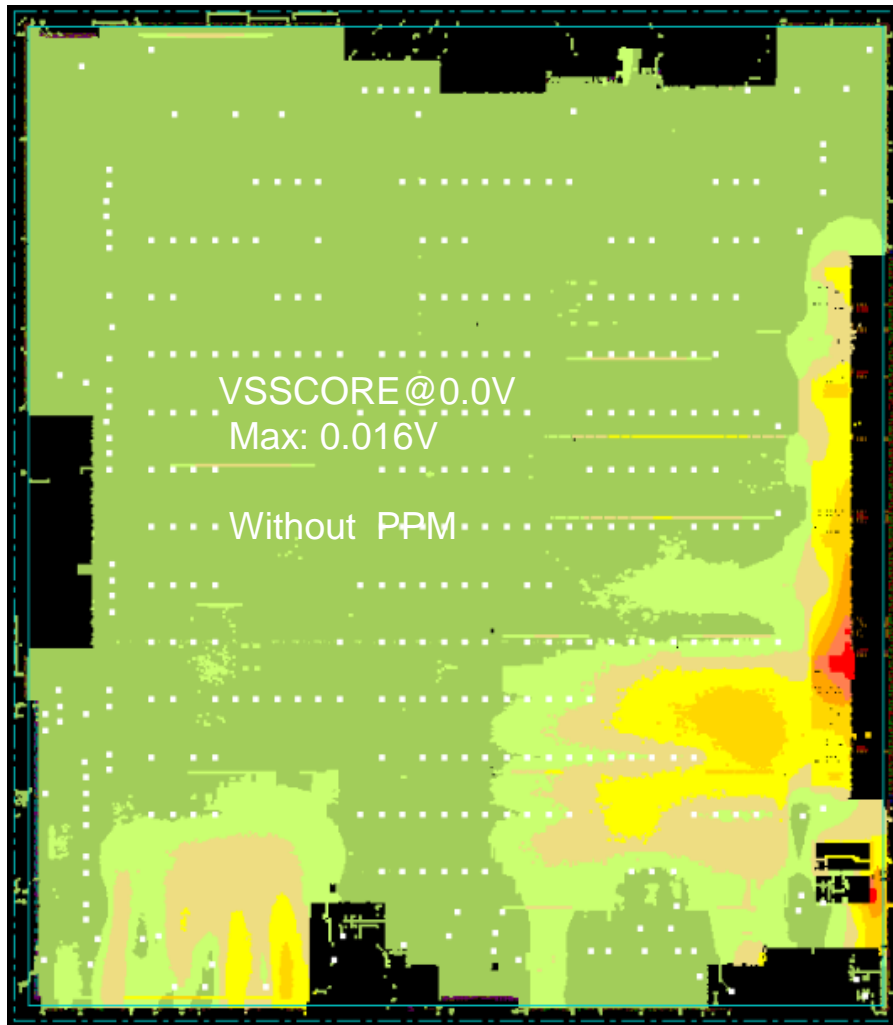
*[Connection Type] DIE

*[Power Nets]

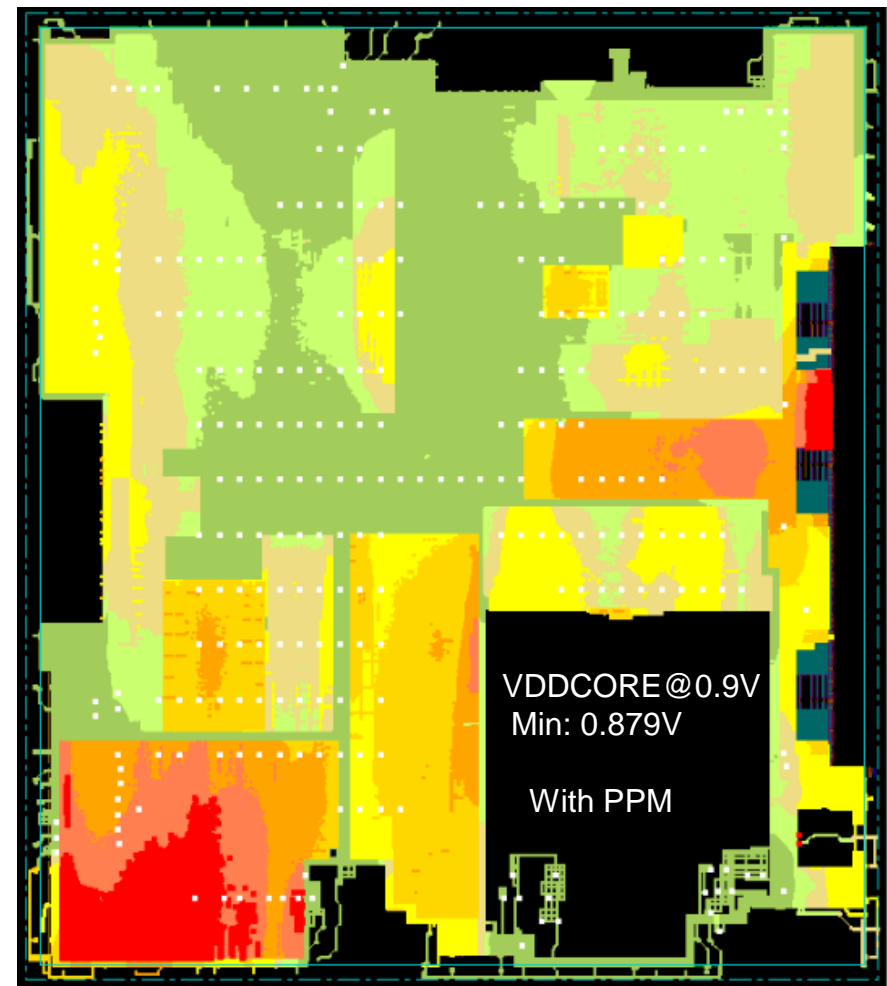
*2	die_top_2	VDDARM	-0.0021476	-0.0022622
*4	die_top_4	VDDARM	-0.0021476	-0.0018622
*5	die_top_5	VDDARM	-0.0021476	-0.0016622

**Total
Distributed**

Chip VSSCORE Static IR-Drop (without and with PPM)



Chip VDDCORE Static IR-Drop (without and with PPM)



Summary

- The new Co-simulation methodology bridge cross domain (Package and IC) database interchange easily and effectively
- DPM model enables to predict more accurate current distribution on each bump pad, week design region and optimize the substrate design before chip tape
- Dynamic IR-Drop with PPM helps to find more real transient voltage and ripple noise, enable IC designer to optimize the on-chip Power Grid design



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Thank You

