Non-correlation of Peak Noise and Peak Current

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Peak Currents and Maximum Noise Amplitude

In a Power Integrity (PI) world dominated by ***i·r drop***, it is common to relate peak noise in a macro power grid with peak current drawn from the supply. After all, if noise is ***i·r***, then peak noise must correspond with peak ***i***, yes? But is this really true? Is a power grid represented with good accuracy as a complicated mesh of resistances? We answer the first part of this exploration – the non-correlation of peak noise with peak current – in this experimental study.

Consider any interconnect segment of a macro block power grid. What are the key aspects of its electrical behavior relevant to PI? It exhibits resistance to the flow of current through it. But it also exhibits electrical inertia, a property termed inductive reluctance, that impedes change in its electrical current flow. And, an electrical capacitance, associated with the wire, reacts to any change in its electric potential. Two of these electrical aspects lead to noise, or variation in its electric potential, while the third helps mitigate it.

The electrical picture isn't all that simple! It's not just a resistance ***r***, though we may like it so.

Equations that capture the behavior of such power grid (PG) interconnect elements aren't simple either. Equation (1) in this 2006 paper represents noise in an interconnect segment, modeled as a *lumped* resistance in series with an inductance, as ***i·r + L·di/dt***. Hidden within this simple relation are more complexities.

Say instantaneous current ***i*** is a sinusoidal wave. That makes the term ***di/dt*** a cosine wave, one shifted in phase by 90° from the original sine. The ***di/dt*** component peaks when the sine wave is rising, or falling, at zero amplitude, and not at the peak of the sine. Besides, ***di/dt*** is zero at the peak of the sine wave. In simple words, peak instantaneous current and the peak rate of change do not coincide. The equation for noise thus combines an in-phase value, ***i·r***, with a 90° shifted value, ***di/dt***, which result does not correlate well with the stimulus in this case.

A *continuum* simulation example lights our way ahead.

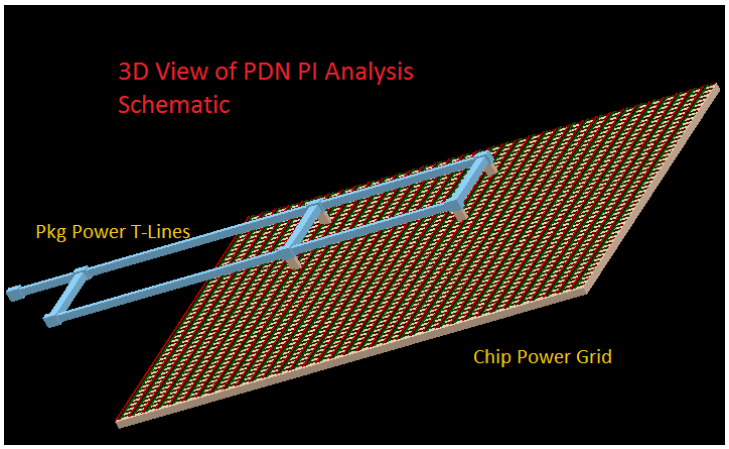

Figure 1: A physical schematic view of a chip power grid and associated PDN

Simulation: Noise Dependency on Load Wave Shape

A chip power grid segment, of ~10mm^2 area, powers a small load current circuit block within. Power pathways from an external supply connect into the chip power grid. The load block sits within an area bounded by terminals connecting to the power grid. **Figure 2** displays electrical properties of the chip grid, and **Figure 1** provides a 3D view.

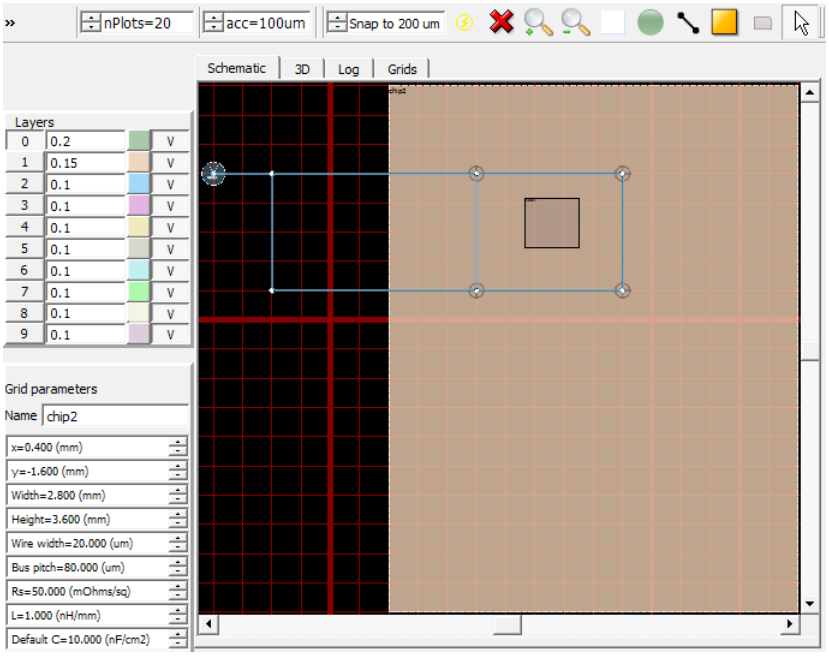

Figure 2: Schematic view of a load current block connecting to a chip power grid and PDN

A true physical electromagnetic solver, PI-FP, **[1]** assists in this experiment. As seen in **Figure 2**, the power grid includes electrical R, L, and C properties of all network components. Moreover, capacitance manifests in a distributed manner in the physical schematic. Impedance and wave propagation characteristics are hence captured as determined by electromagnetic behavior. This simulation environment provides ***continuum modeling*** of PG interconnect, which is a maximal extension of distributed modeling.

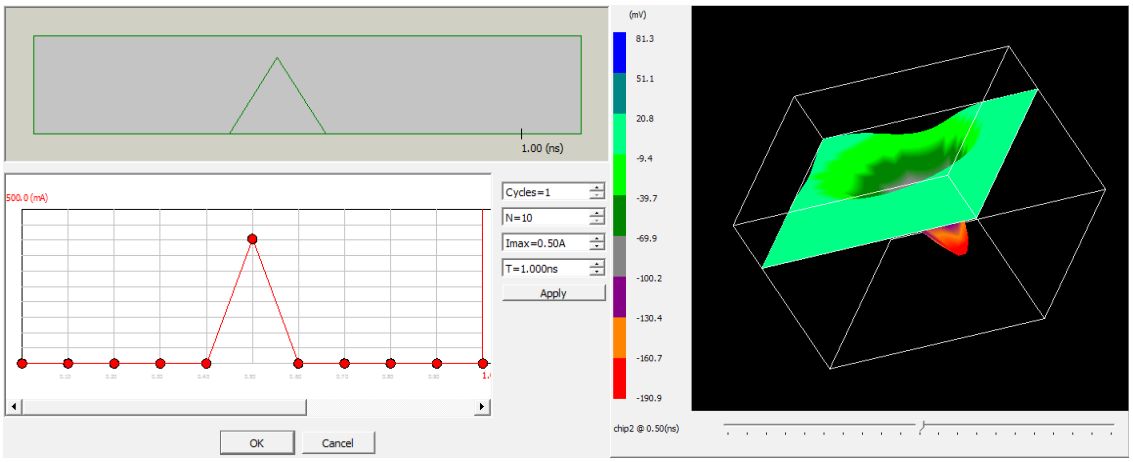

Figure 3: Triangular load current shape and chip noise

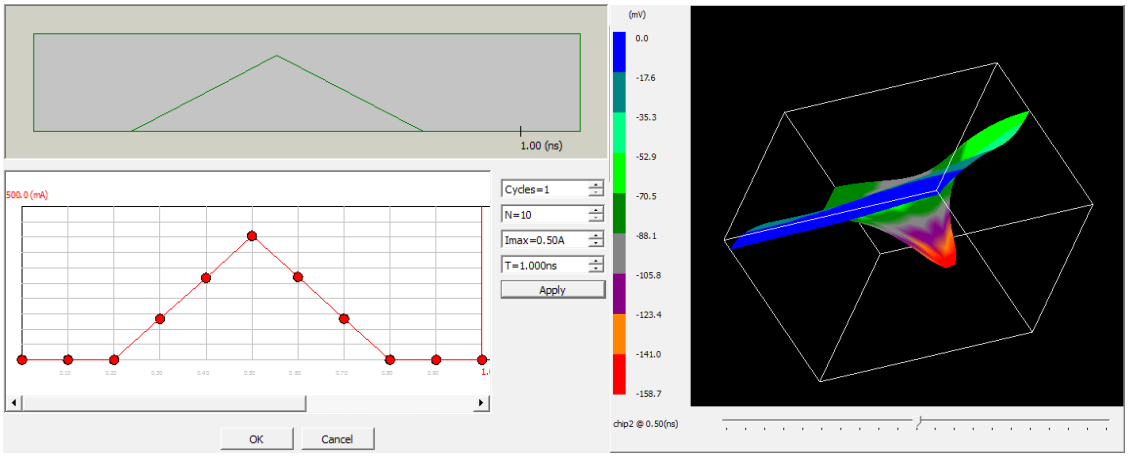

Figure 4: Low *di/dt* triangular load wave and chip noise

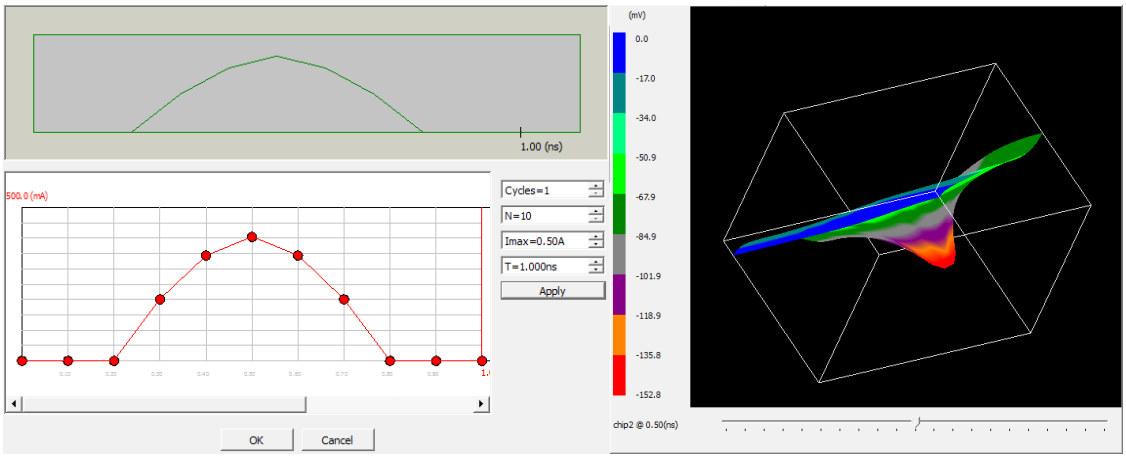

Figure 5: Half-Sine load current wave and chip noise

The chip power grid comprises 1nF of distributed capacitance. The load block provides capacitance in its active circuits, which sums up to ~100pF. Transmission lines of substantial inductance value connect to an external power supply. Hence, in this experiment, it is the local and distributed capacitance that provides charge drawn by the load.

The experiment varies load current shape, changing its slope, spectral components, and per-cycle-charge. Peak load current amplitude remains 400mA for all three cases studied.

Results

The baseline load of 400mA 200ps triangular wave produced peak DVD of 191.7mv as in **Figure 3**. Peak noise correlated in time with peak current in this case, though this observation is limited by the snapshot time resolution of 100ps. **Figure 4** shows reduced peak noise with a 400mA 600ps triangular wave. In this case, *di/dt* reduced by 3X, and peak DVD was 158.7mV. Note that charge consumed has increased by 3X, corresponding to the widening of the triangular base. Thus, the benefit of reduced *di/dt* far exceeded any impact of increased charge draw here. **Figure 5** illustrates a further reduction in noise to 153.4mV despite more increase in charge consumption. The half-sine load current wave improved upon the triangular shape in changing the overlap of resistive and reactive noise components.

All three cases employed peak load current of 400mA, changing only load wave shape. Thus peak noise amplitude shows no correlation with peak current in this experiment. Peak noise also shows no correlation with maximum power consumption proportional to the area of the current waves.

One may rightly ask: is *peak noise amplitude* a true measure of overall PI degradation?

[1] PI-FP True physical PI simulator, Anasim Corp. (http://anasim.com/pi-fp/pifp.htm)

Raj Nair is the founder of Anasim Corp. and a consultant with 25+ years in Electronics and IC Design. He specializes in Power Integrity (PI) analysis and management for chips and systems, an emerging area of importance to integrated system design. He has authored/edited two engineering books in Power Integrity, and holds 40+ US and International patents. He is occupied at present with PI Consulting and commercializing Anasim's PI-FP technology. His interests include start-up efforts and publishing mainstream nonfiction books.

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